



CEIUPM

Centro de
Electrónica
Industrial

Analysis of a Heterogeneous Multi-Core, Multi-HW-Accelerator-Based System Designed Using PREESM and SDSoC

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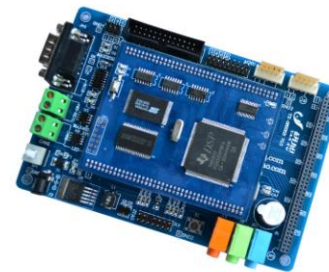


POLITÉCNICA

Introduction

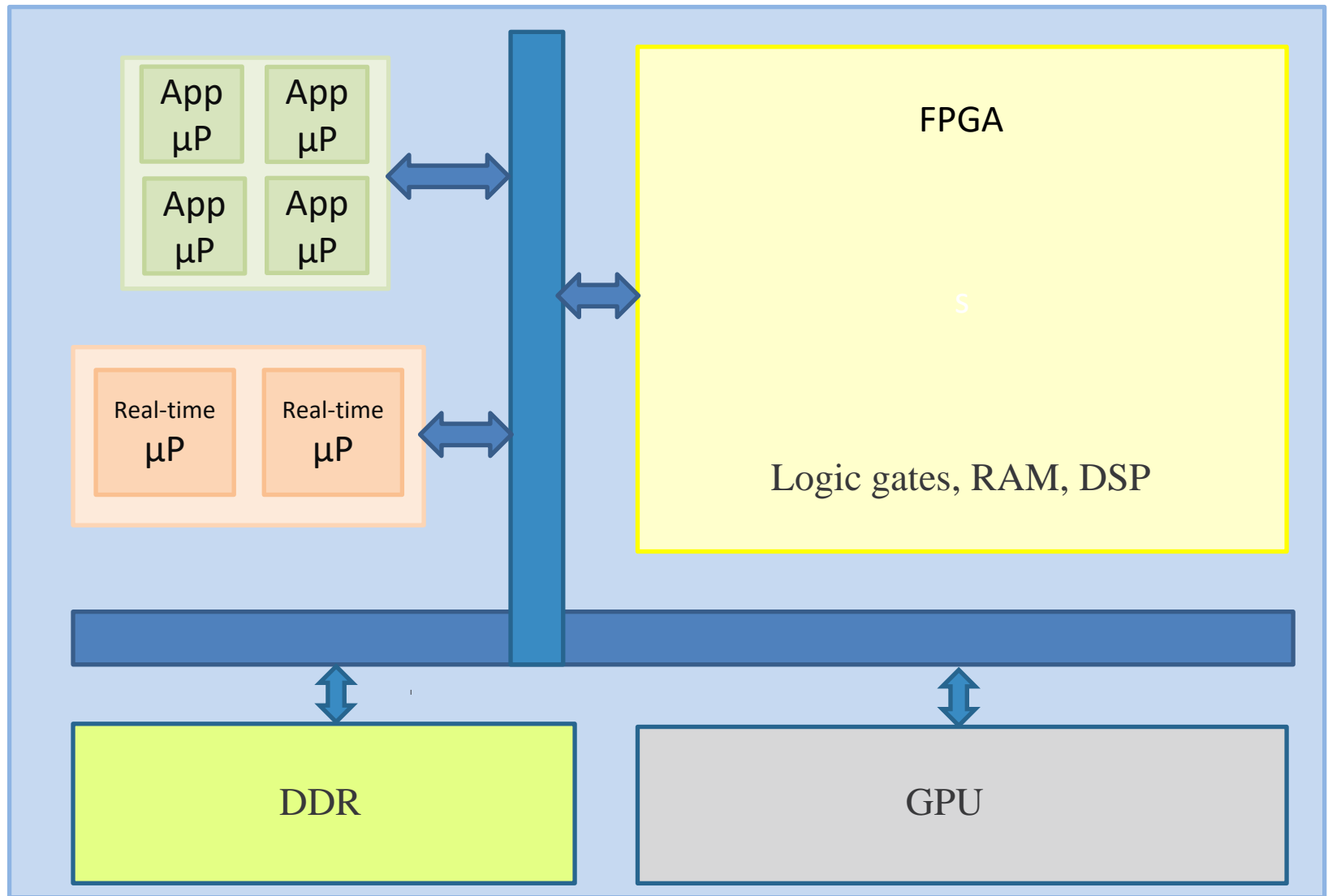


Embedded
World

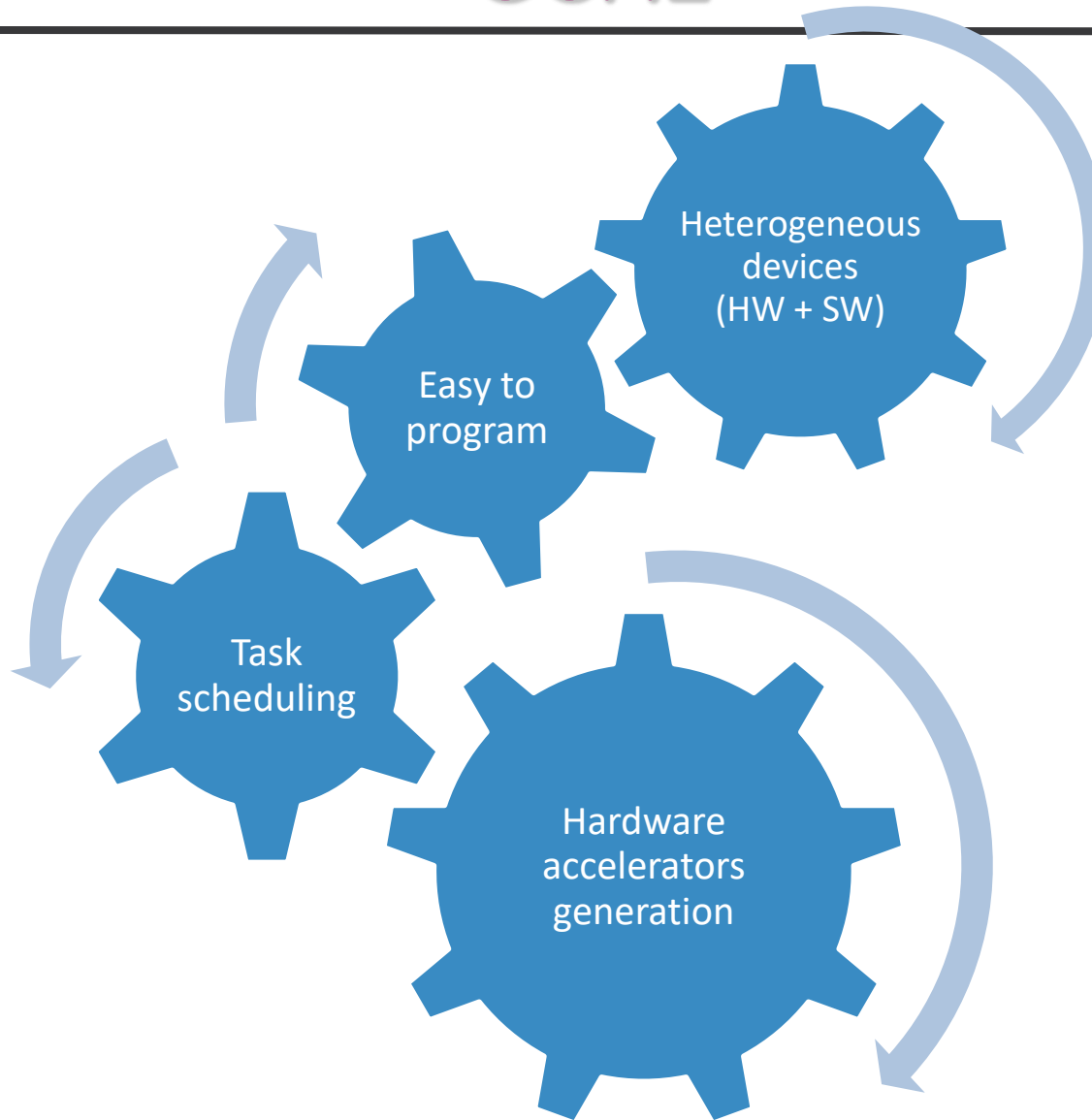


...and many others

Heterogeneous devices

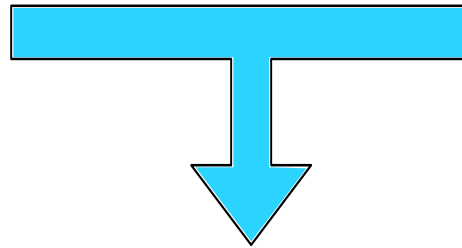


GOAL



...method for fast
prototyping and
DSE

Used Tools



Rapid prototyping of software applications enabling:

- deadlock-free code generation using **PiSDF MoC**
- custom **hardware acceleration** and generation

Video Processing Application



Sobel



Original Image

Split



Slices

Process

Process

Process



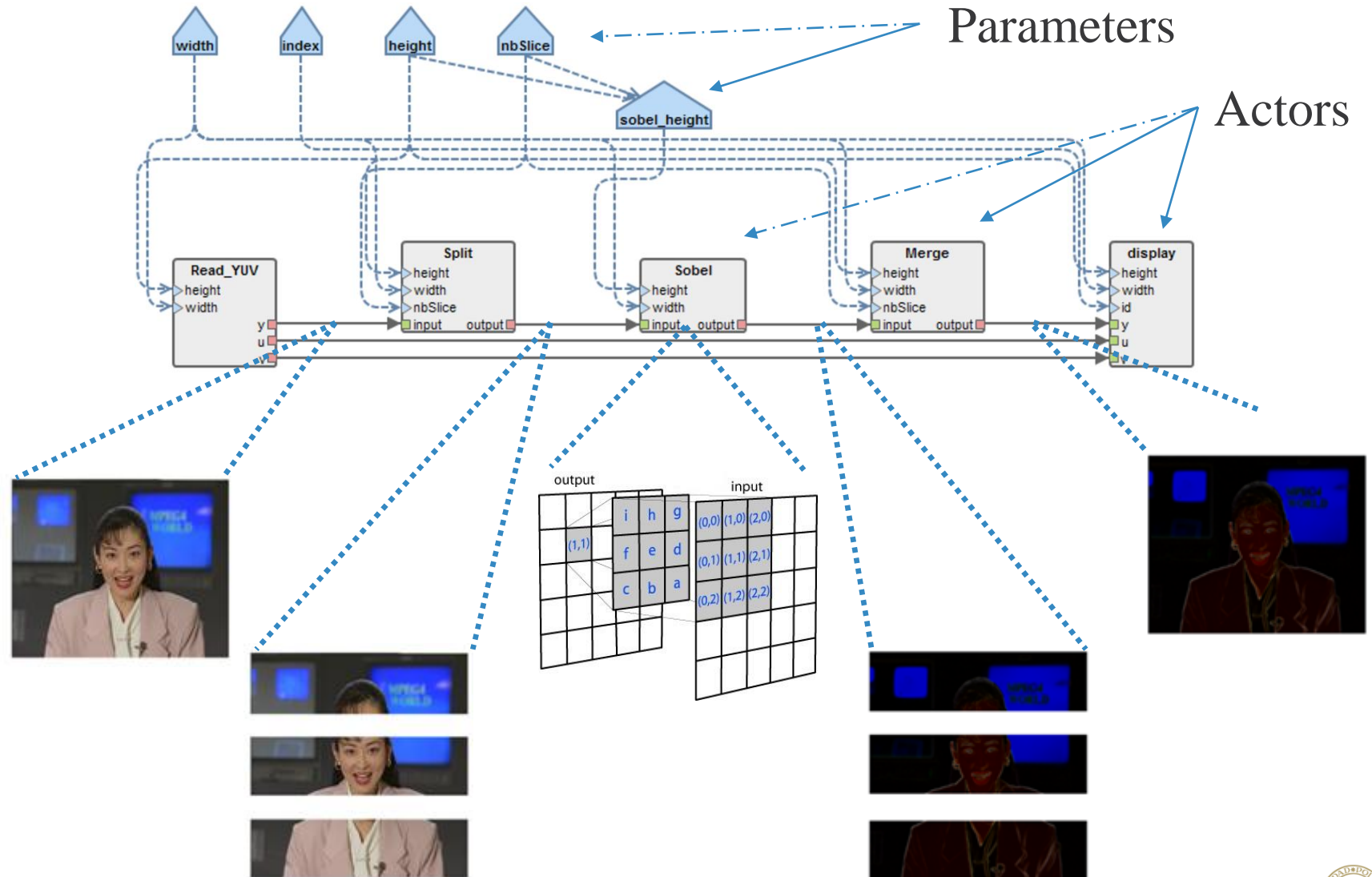
Filtered Slices

Merge



Filtered Image

Actors Specification



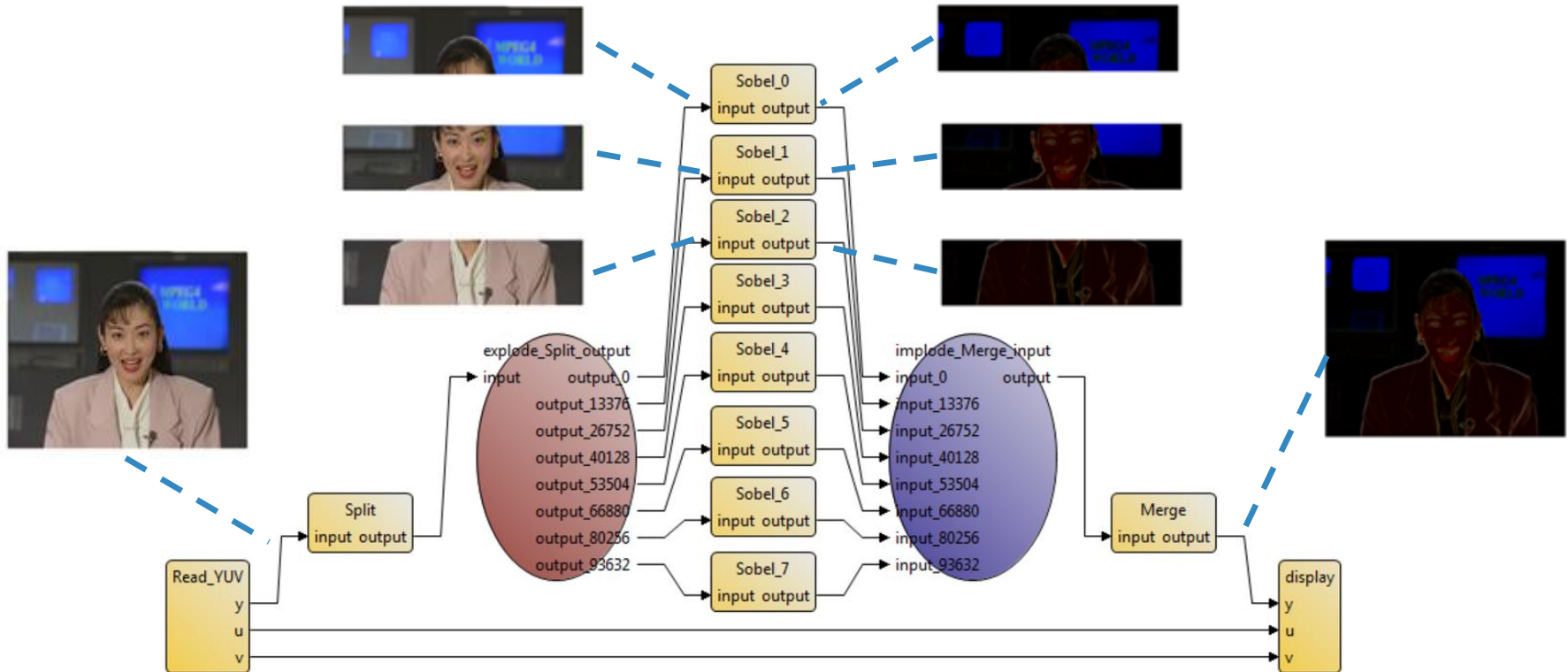
COWOMO



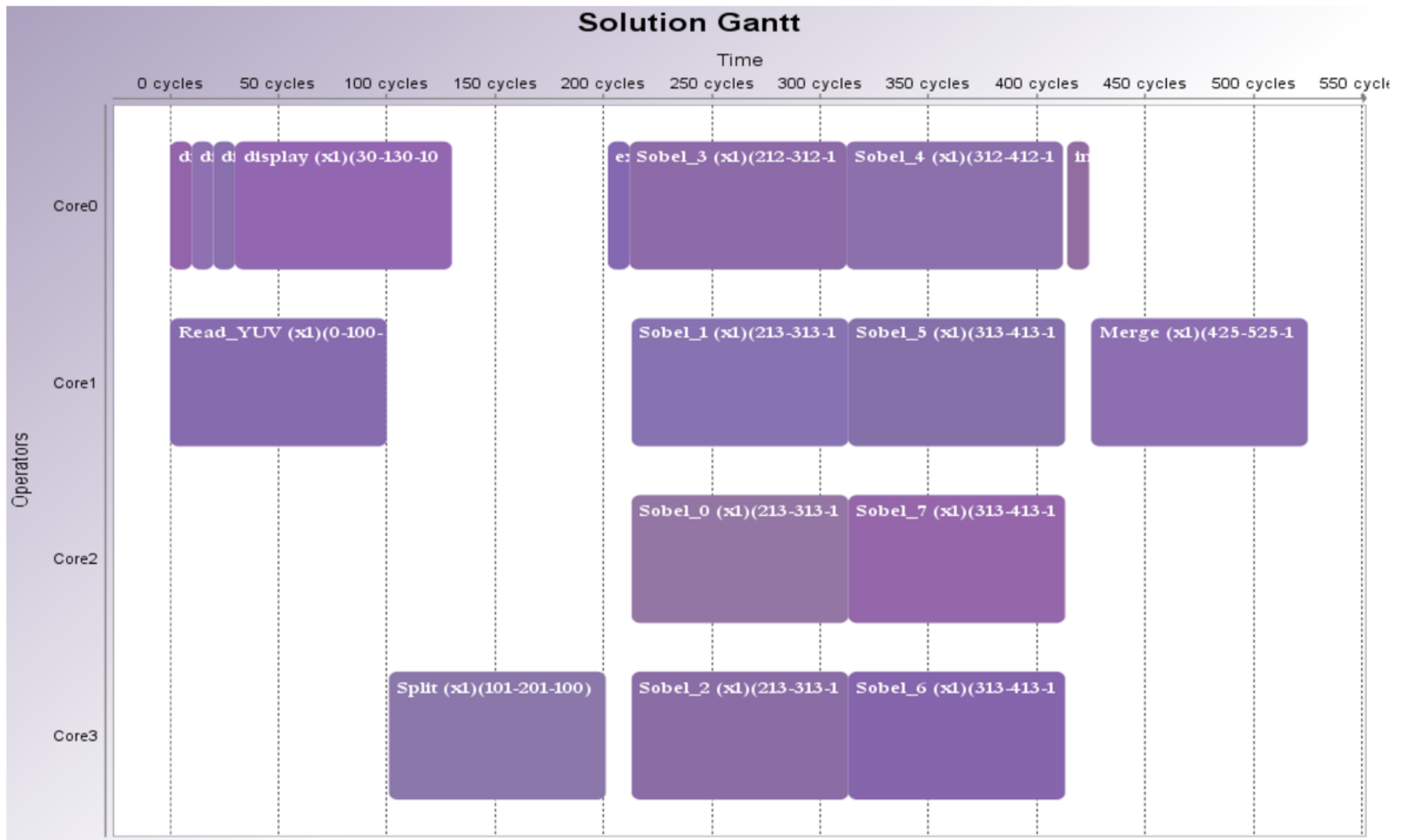
2018

Exposed parallelism

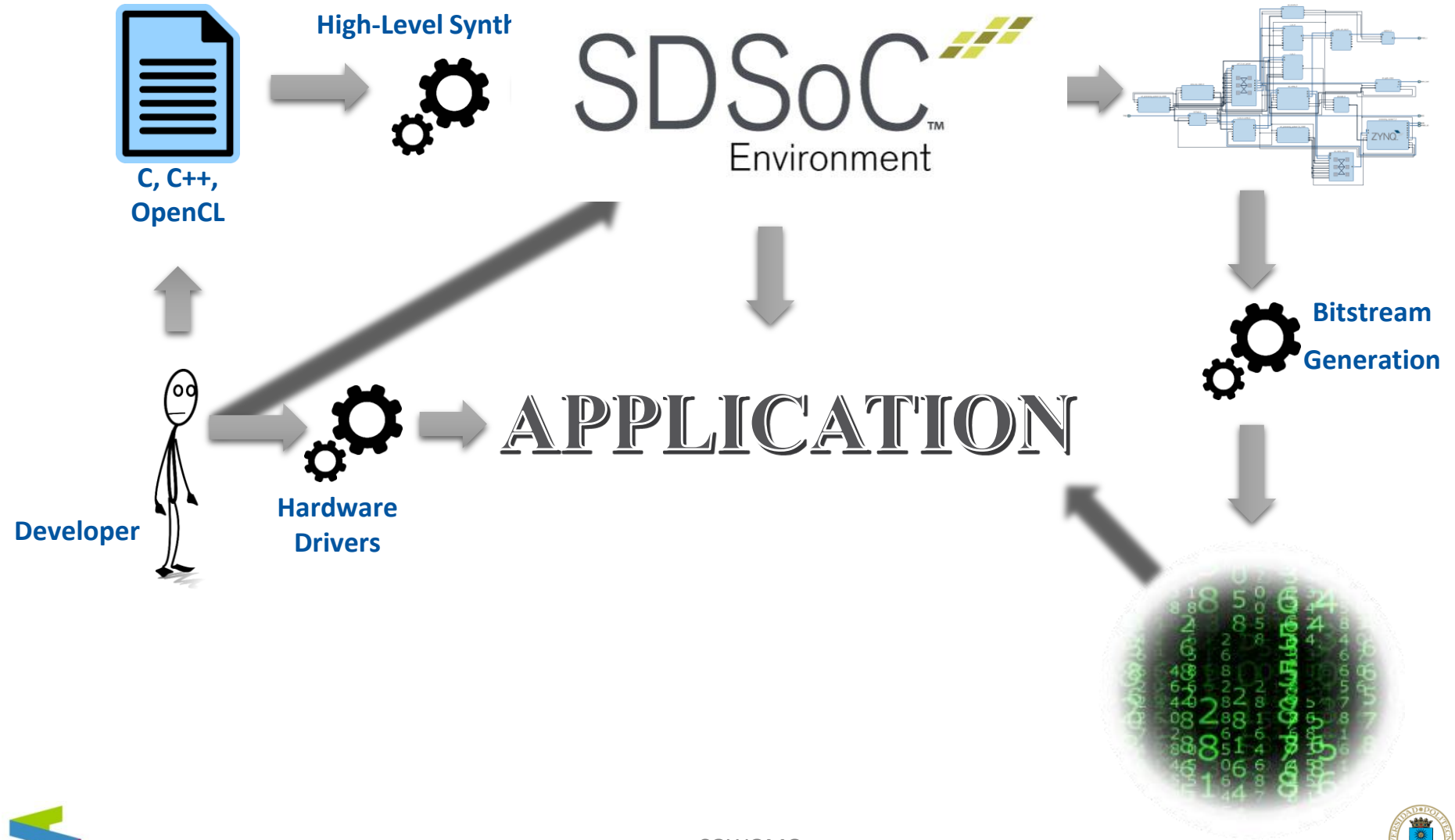
Equivalent single-rate graph where each edge has equal production and consumption rates of token.



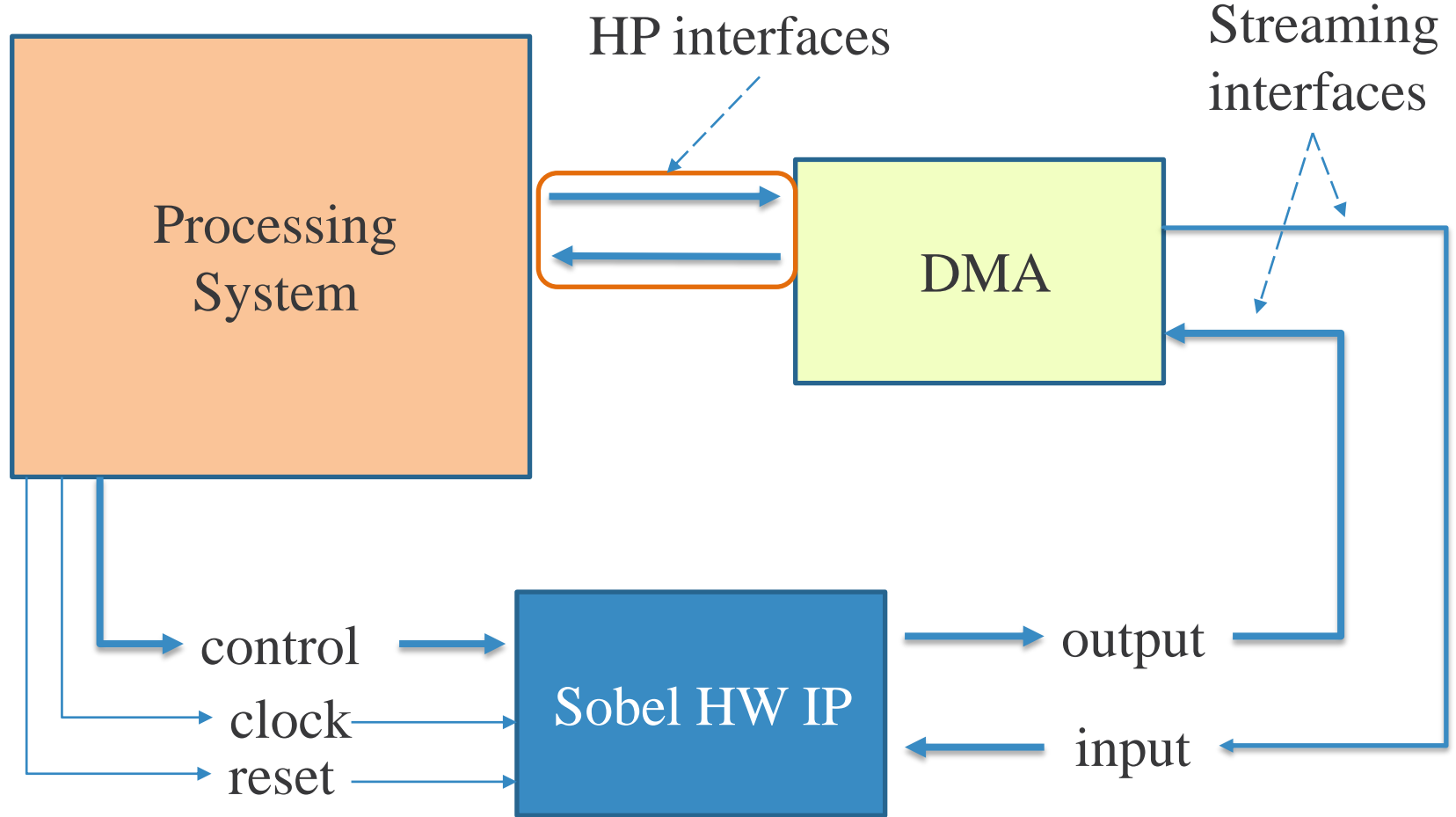
Actors scheduled



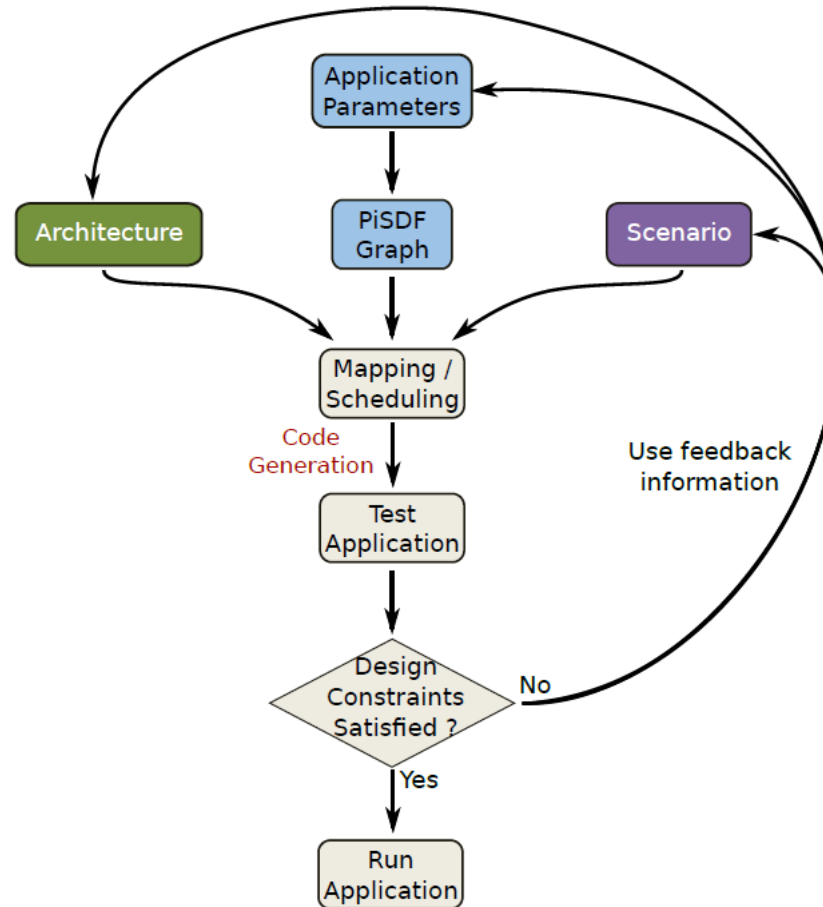
High Level Synthesis and SDSoC



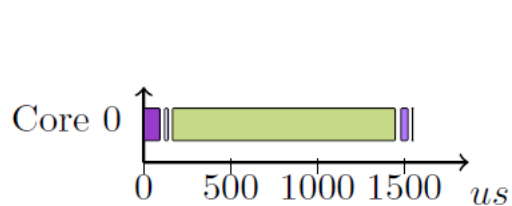
From PREESM to SDSoC



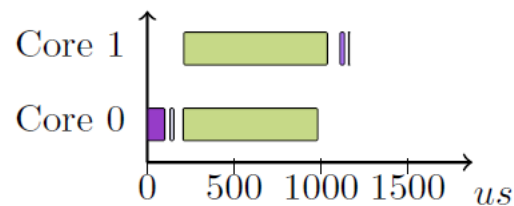
Design Space Exploration



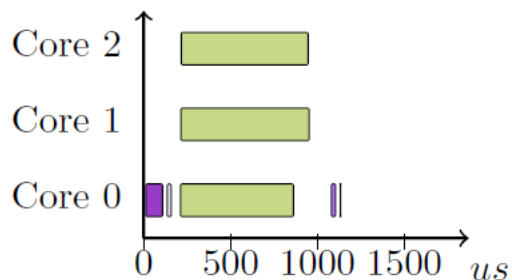
Results on Ultrascale+ (static)



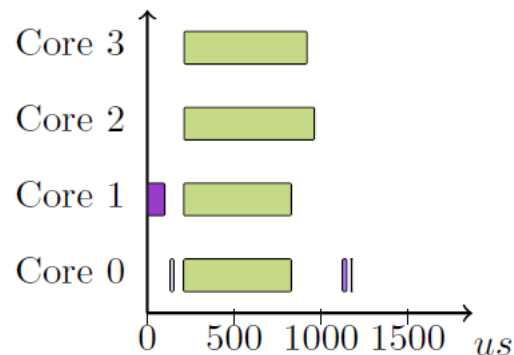
(a)



(b)



(c)

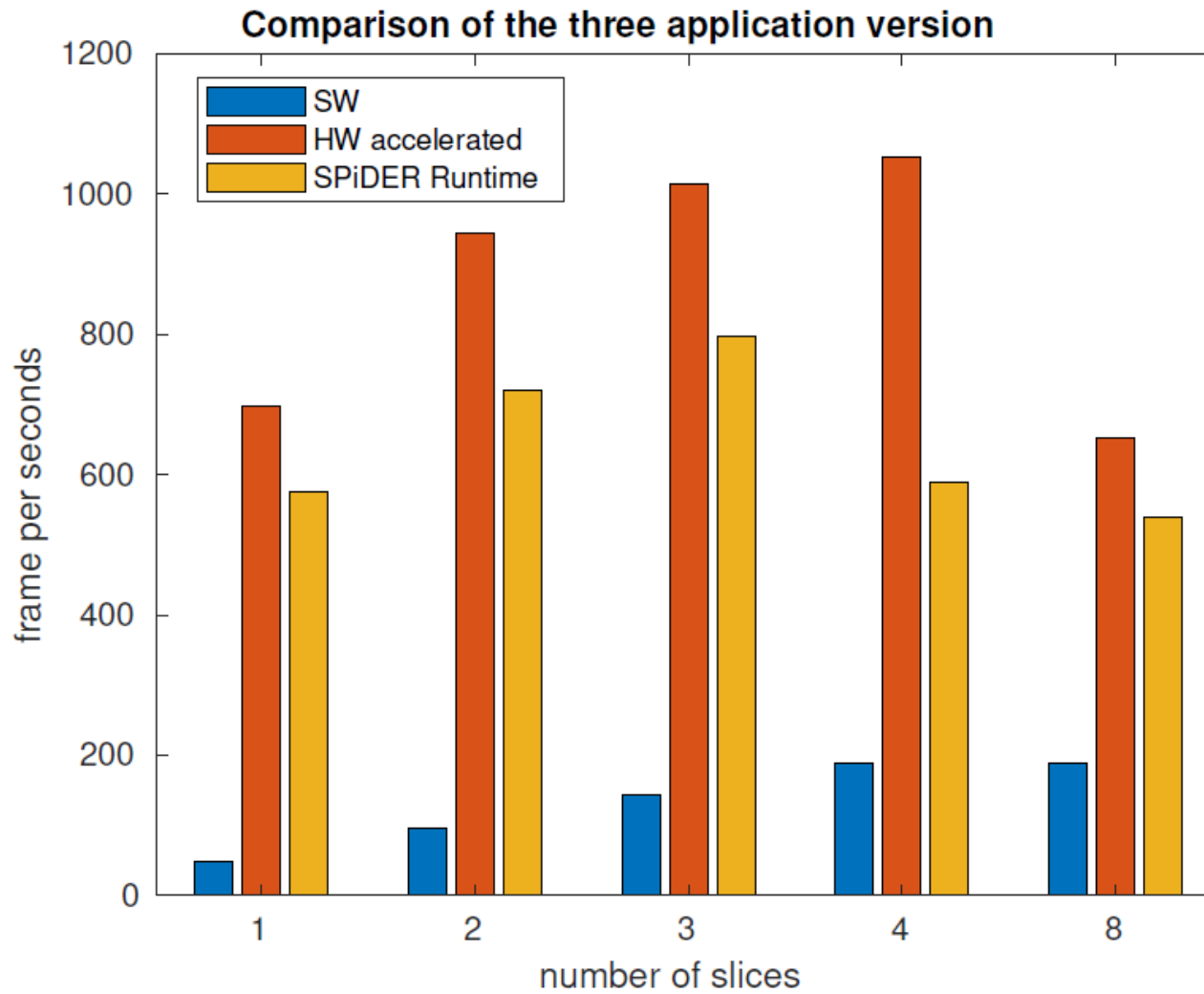


(d)



(e)

Comparison



Results on Ultrascale+ (runtime)



Thank you for your attention