Horizon 2020
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CERBERO

MDC Tutorial

CGR Coprocessor Generation from Dataflow Networks

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Outline

- Introduction
  - HW Reconfigurability
  - Dataflow to Hardware
- MDC Tool
- Tutorial Details
  - Sobel and Roberts Operators
  - Operator Dataflow Descriptions
  - Tutorial Steps
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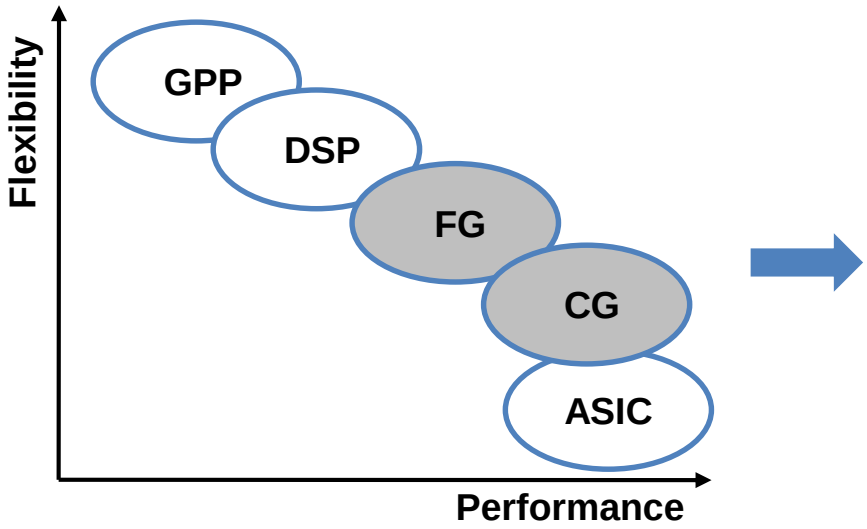
Hw Reconfigurability

Fine-Grain Reconfiguration

- High flexibility bit-level reconfiguration
- Slow and memory expensive configuration phase

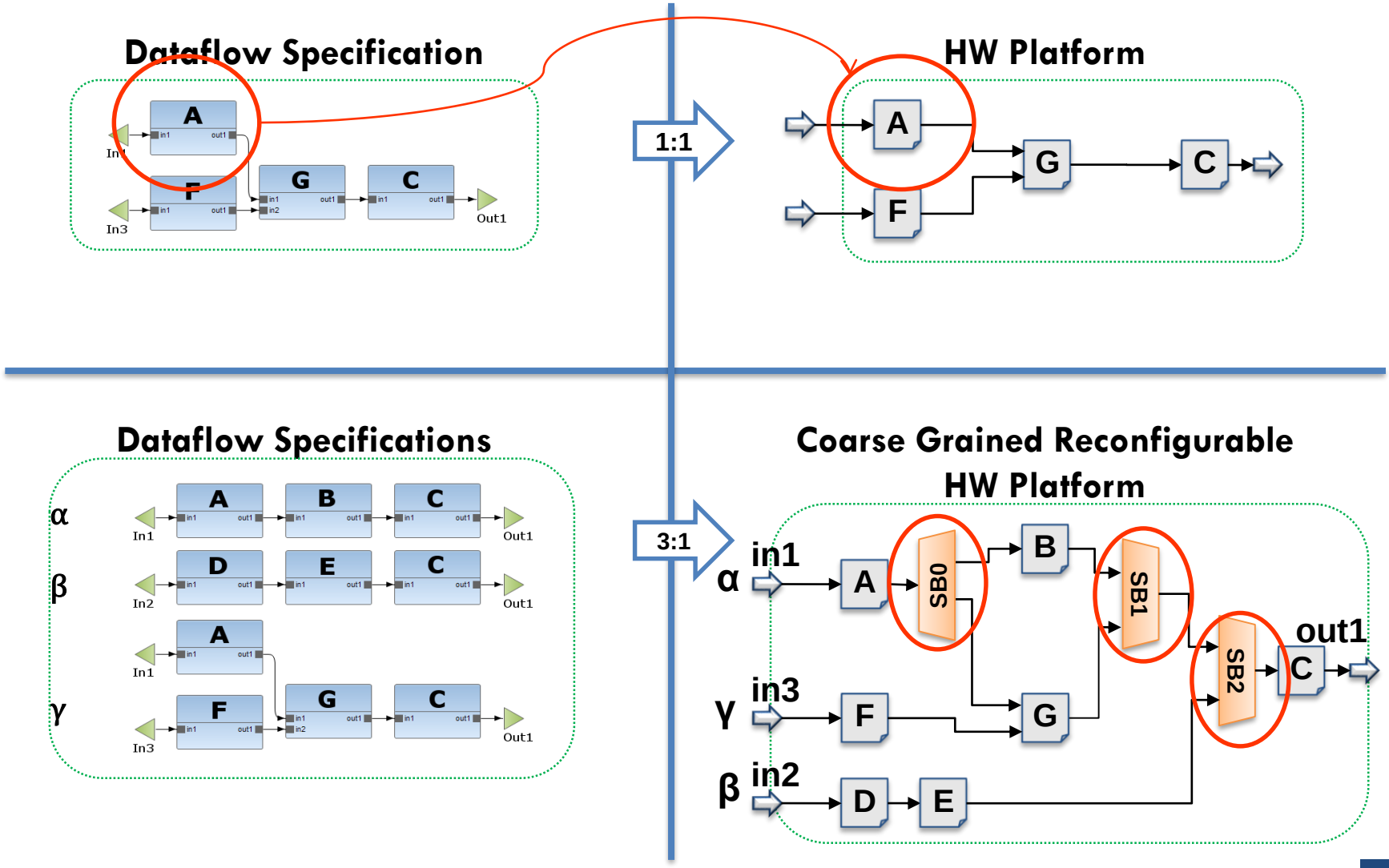
Coarse-Grain Reconfiguration

- Medium flexibility word-level reconfiguration
- Fast configuration phase

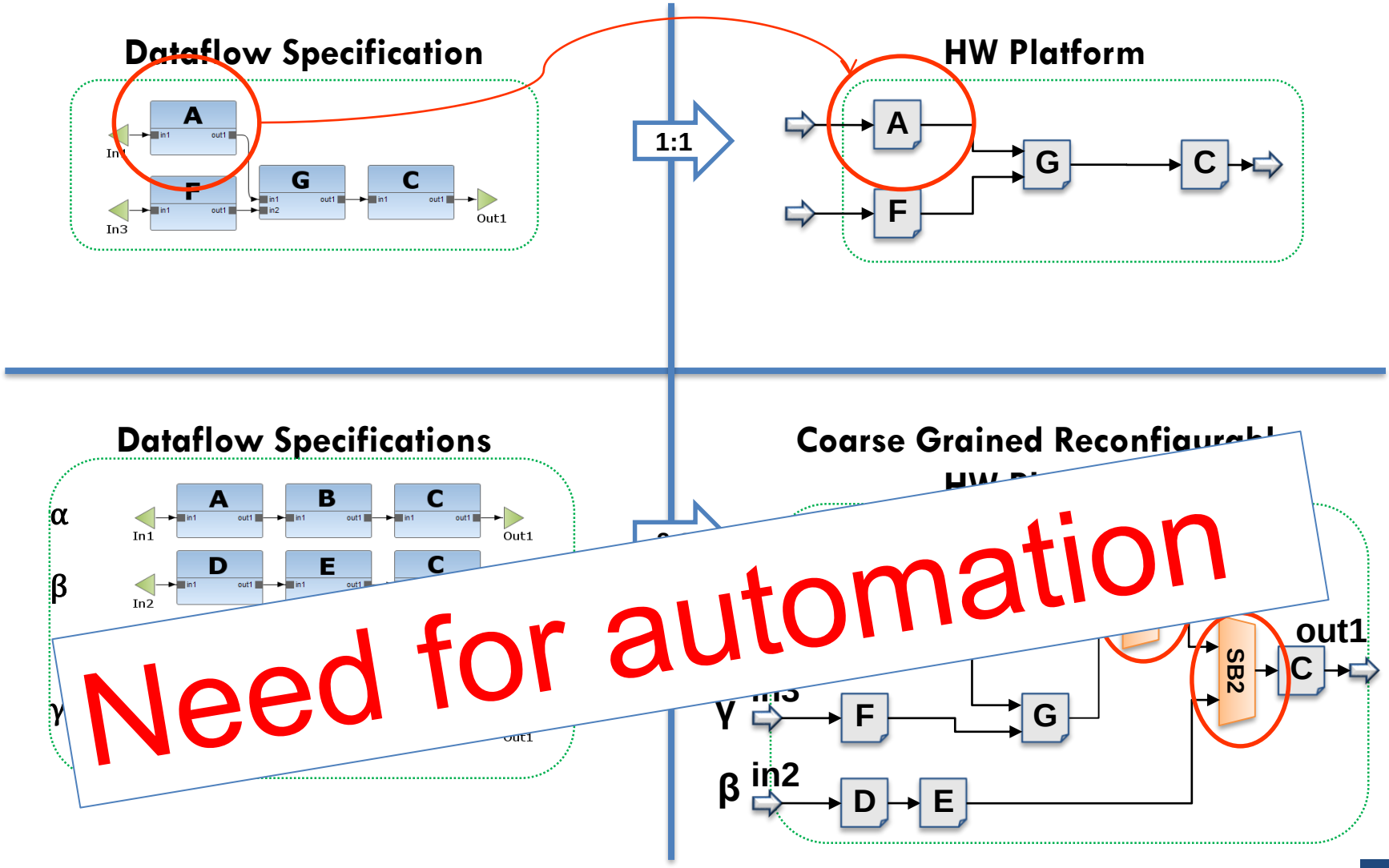


	FG	CG
	Bit-level	Word-level
Flexibility	☺	😐
Reconf. Speed	😐	☺
Config. Storage	☹	😐

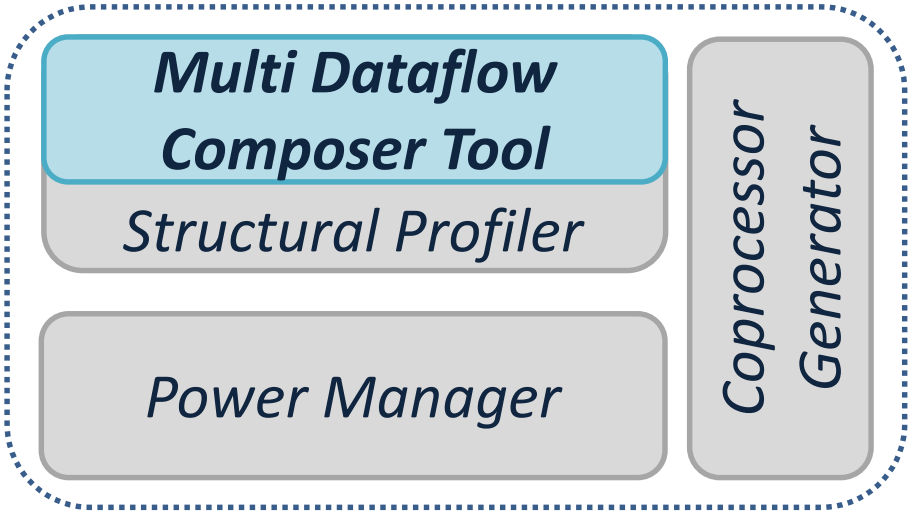
Dataflow to Hardware

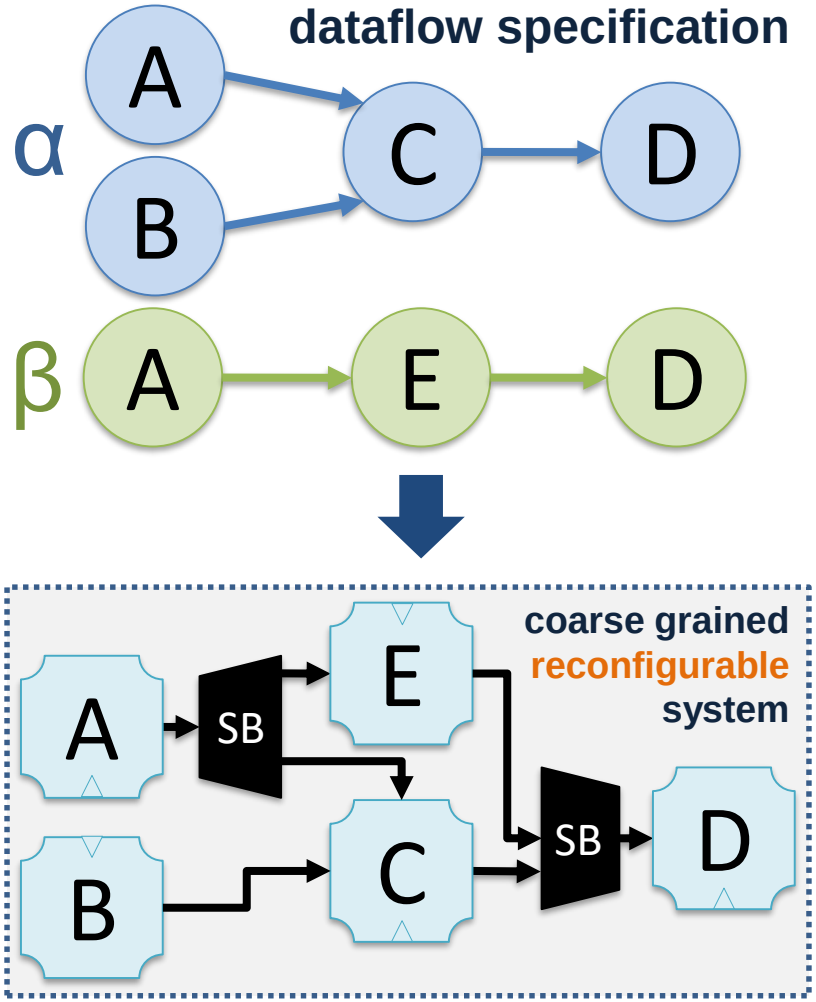


Dataflow to Hardware



Multi Dataflow Composer Tool

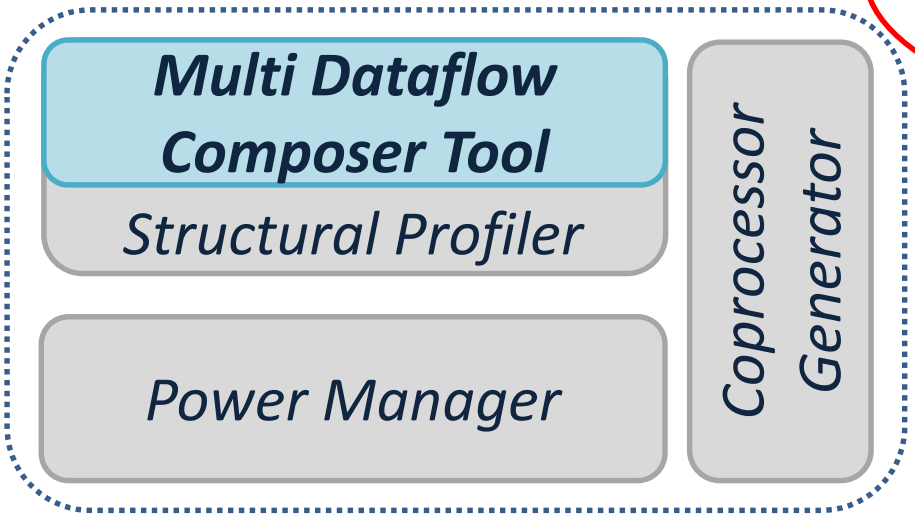


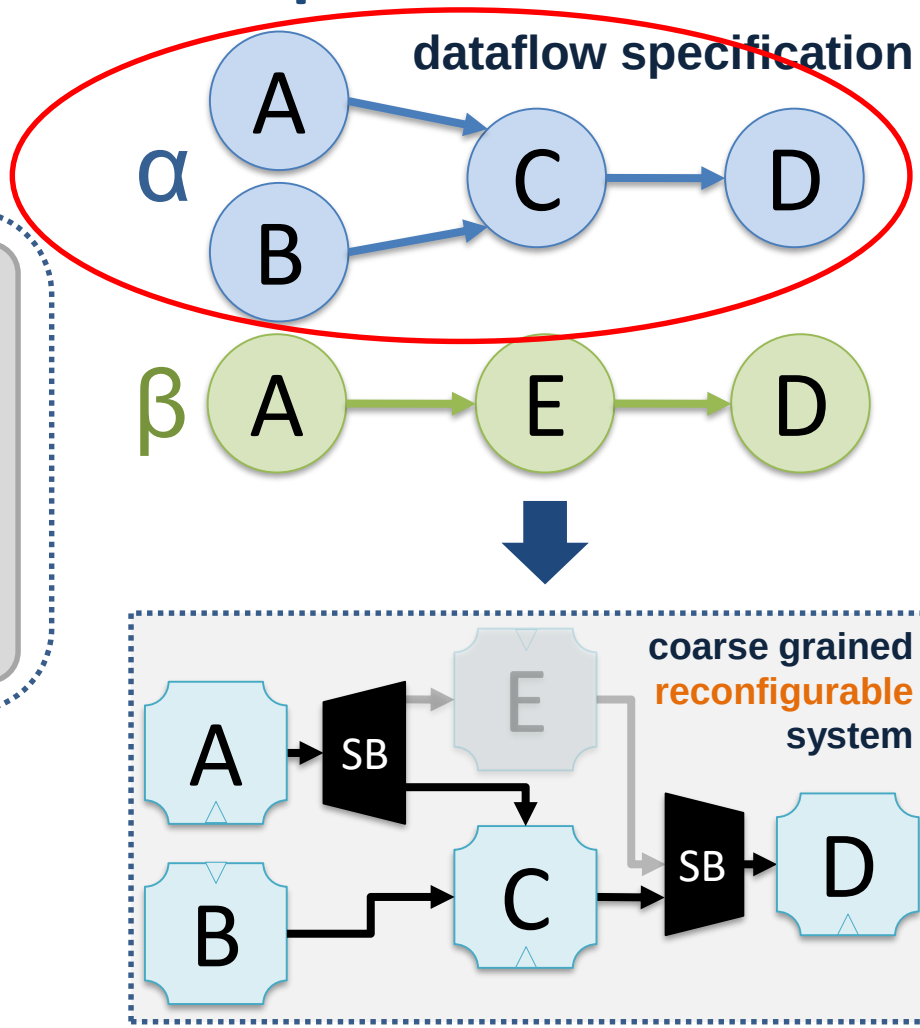


MDC design suite

http://sites.unica.it/rpct/

Multi Dataflow Composer Tool





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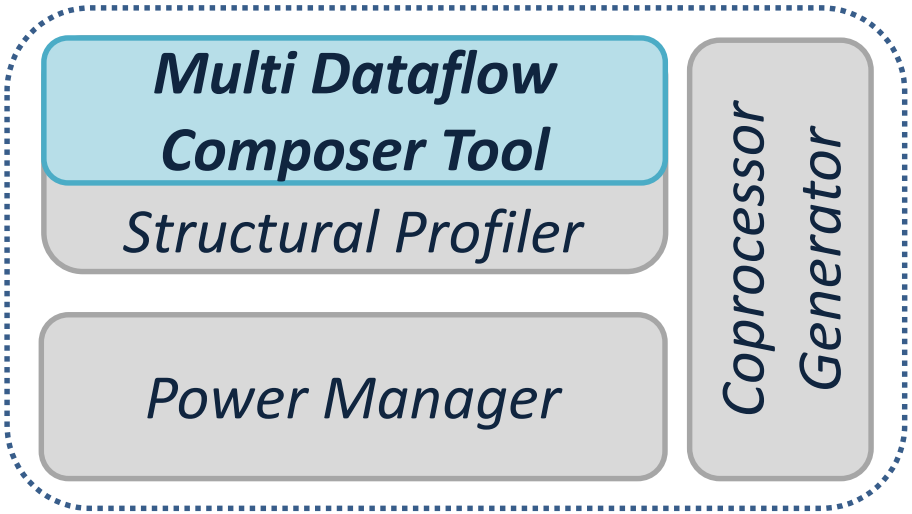

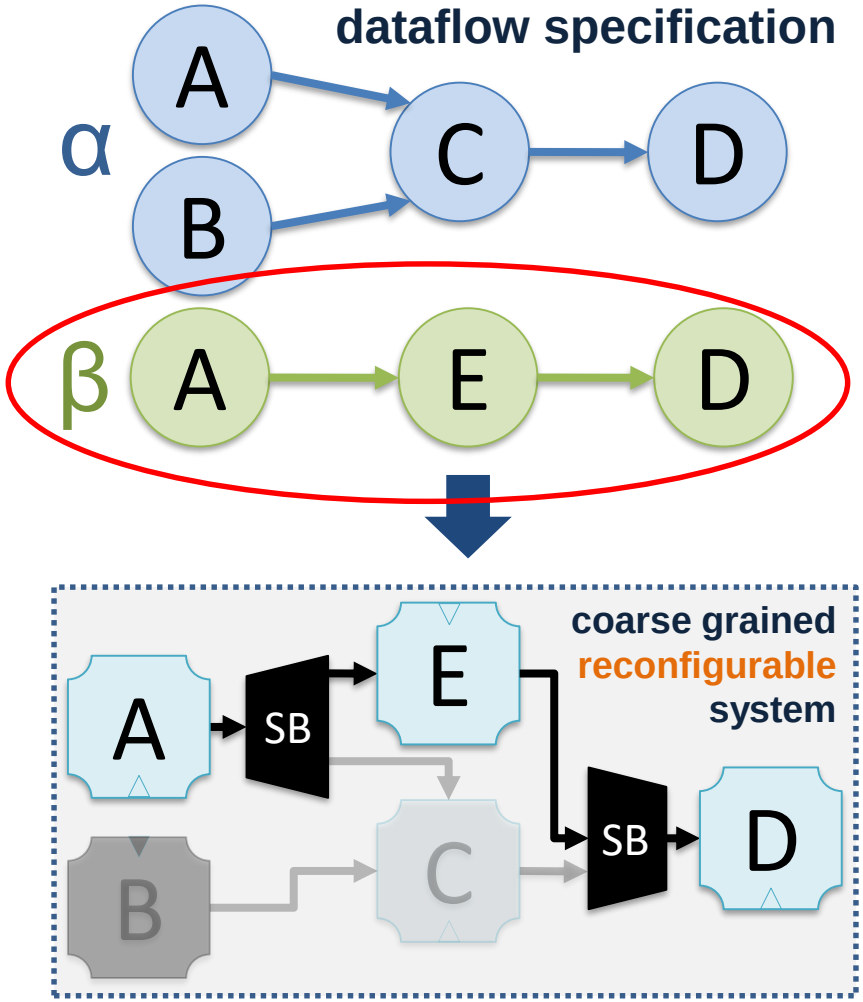

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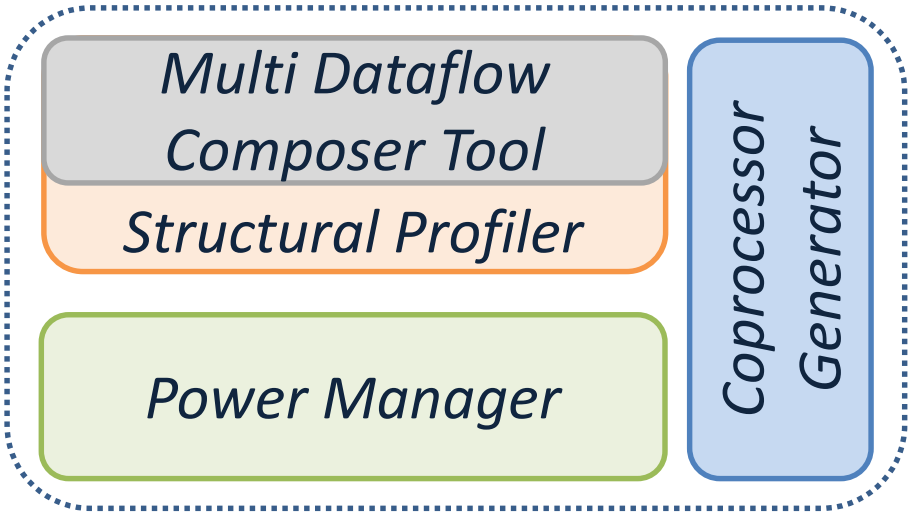

MDC design suite

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Structural Profiler:

low-level feedback (from synthesis) and DSE for topology optimization.

- (ASIC + FPGA)

Coprocessor Generator:

generation of ready-to-use Xilinx IPs

- (FPGA)

Power Manager:

automatic application of clock-gating and/or power-gating.

- CG (ASIC + FPGA)
- PG (ASIC)

Multi Dataflow Composer Tool

Multi Dataflow Composer Tool

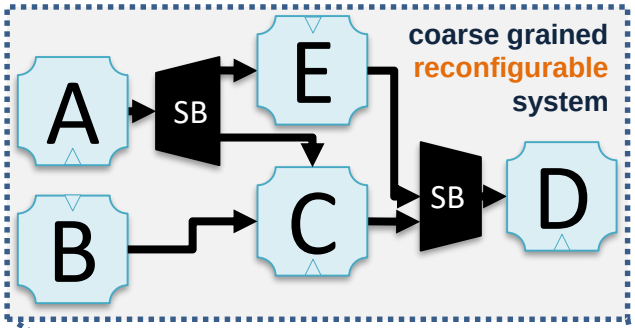
Structural Profiler

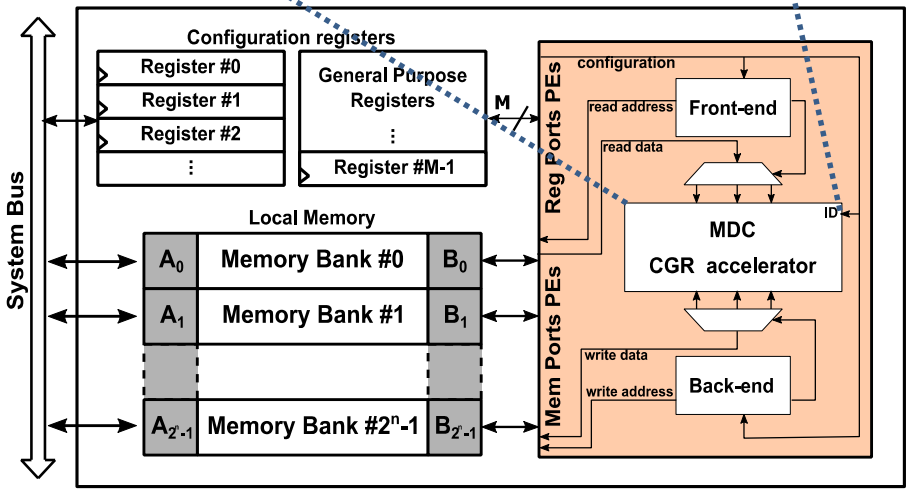
Power Manager

Coprocessor Generator

Coprocessor Generator:

generation of ready-to-use Xilinx IPs





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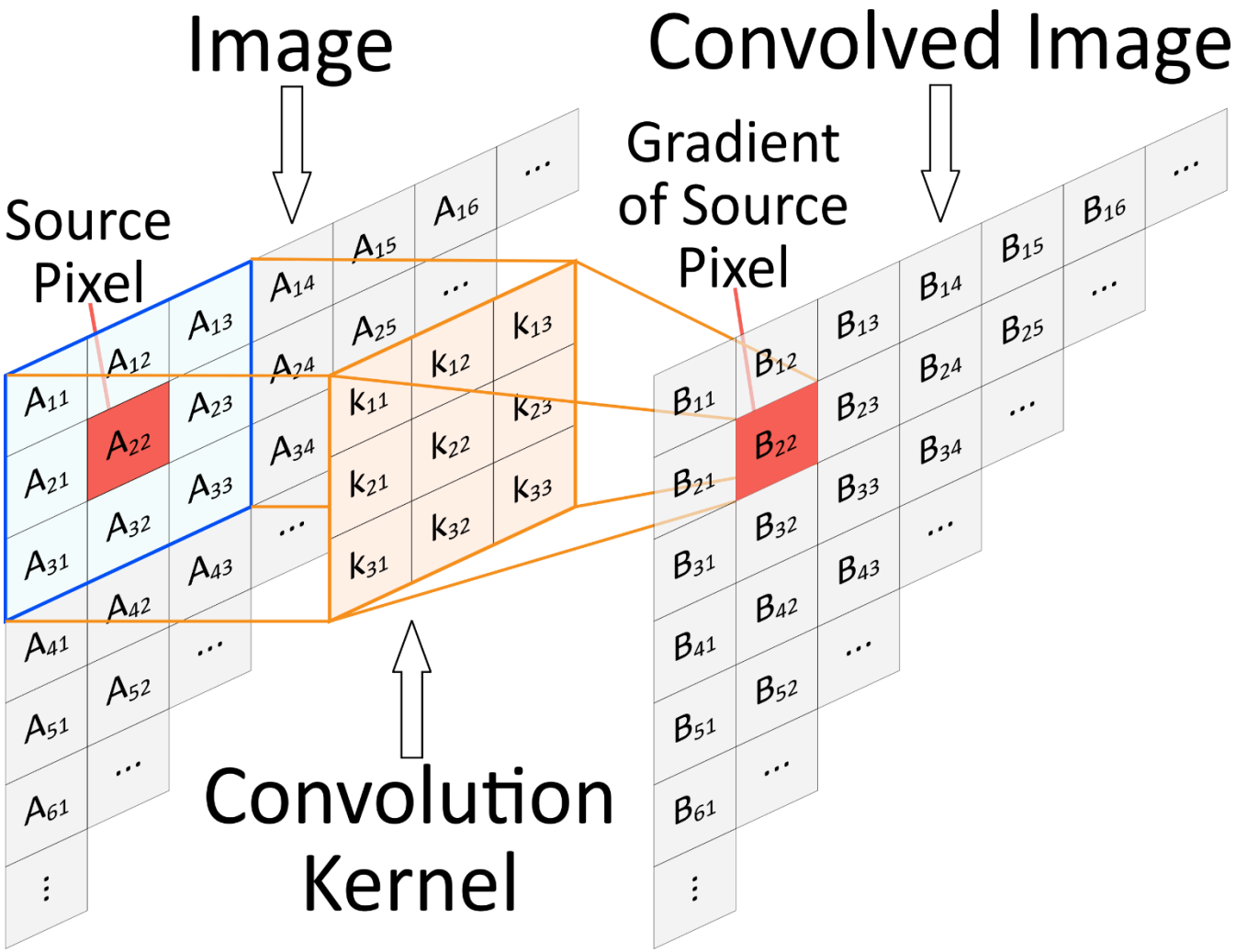
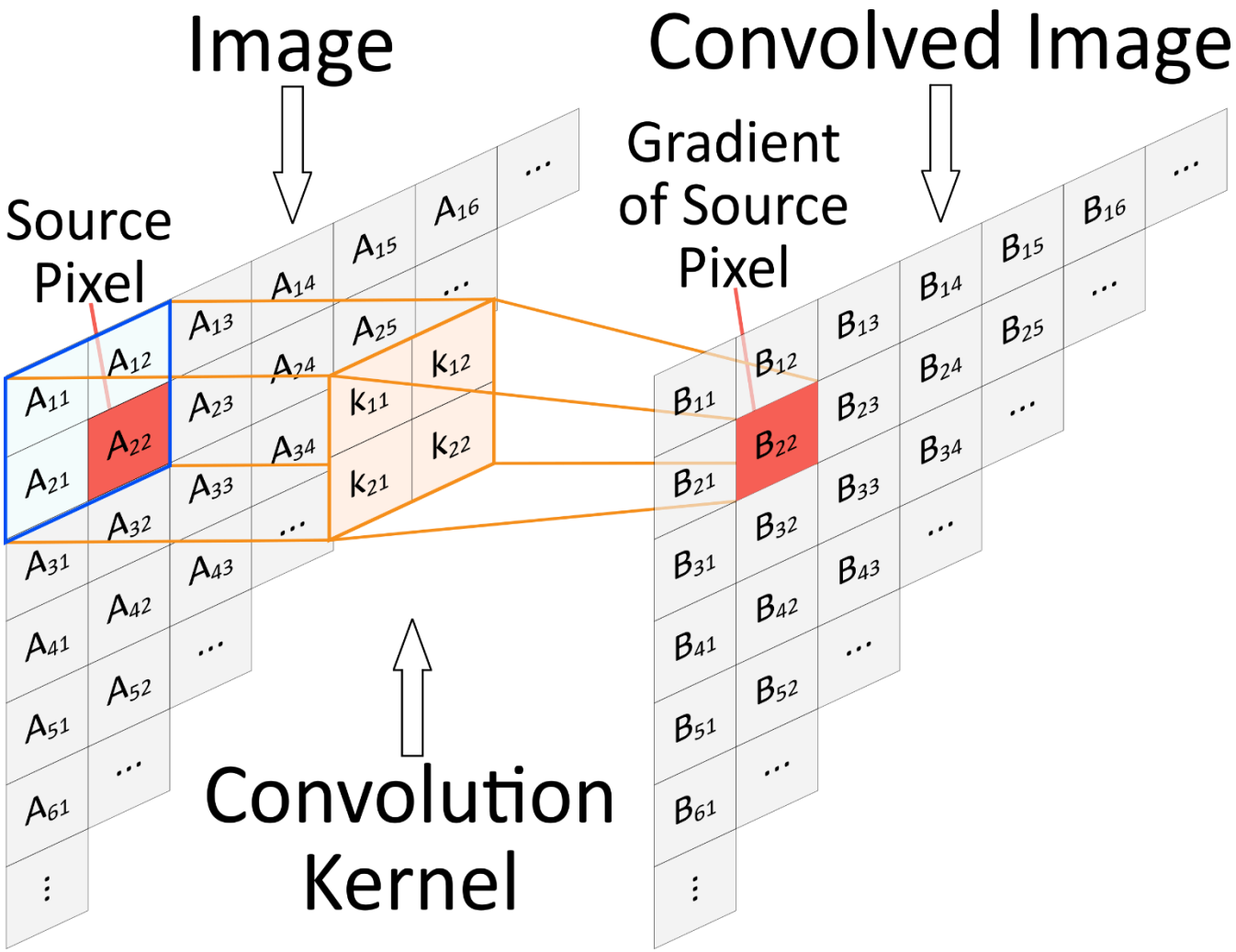
Sobel Operator

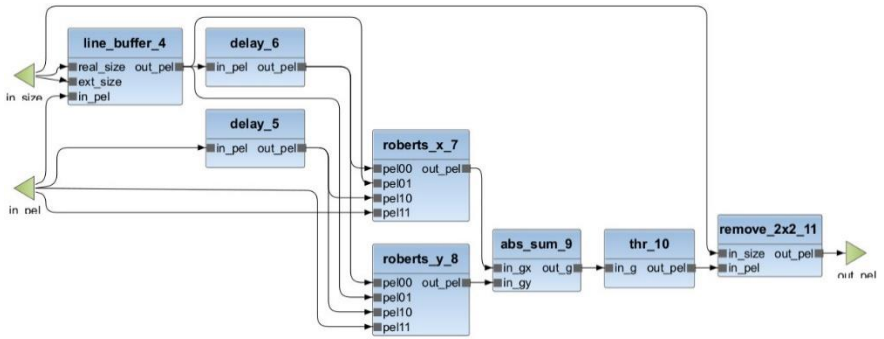


Roberts Operator

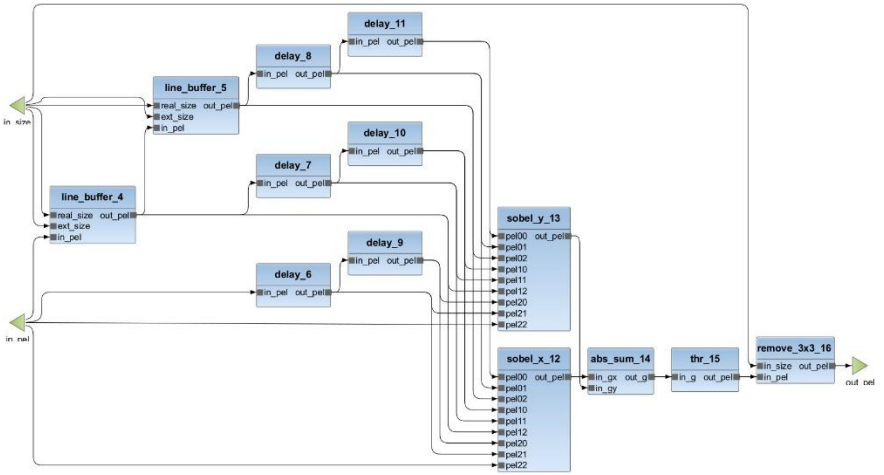


Operators Dataflow Descriptions

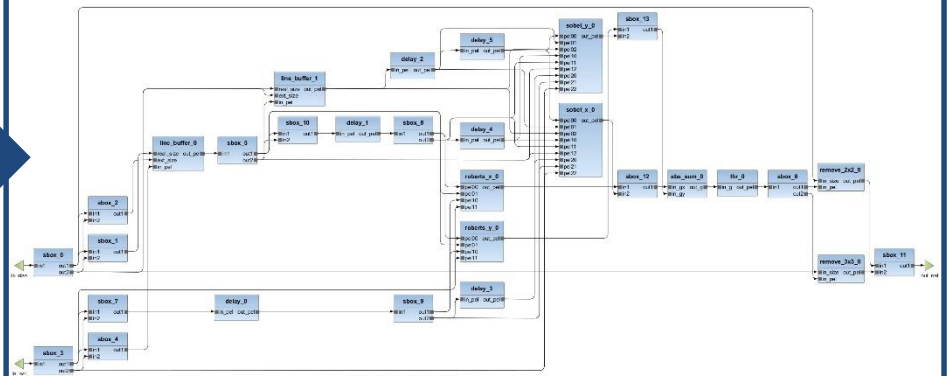
Roberts network



Sobel network



Multi-dataflow network

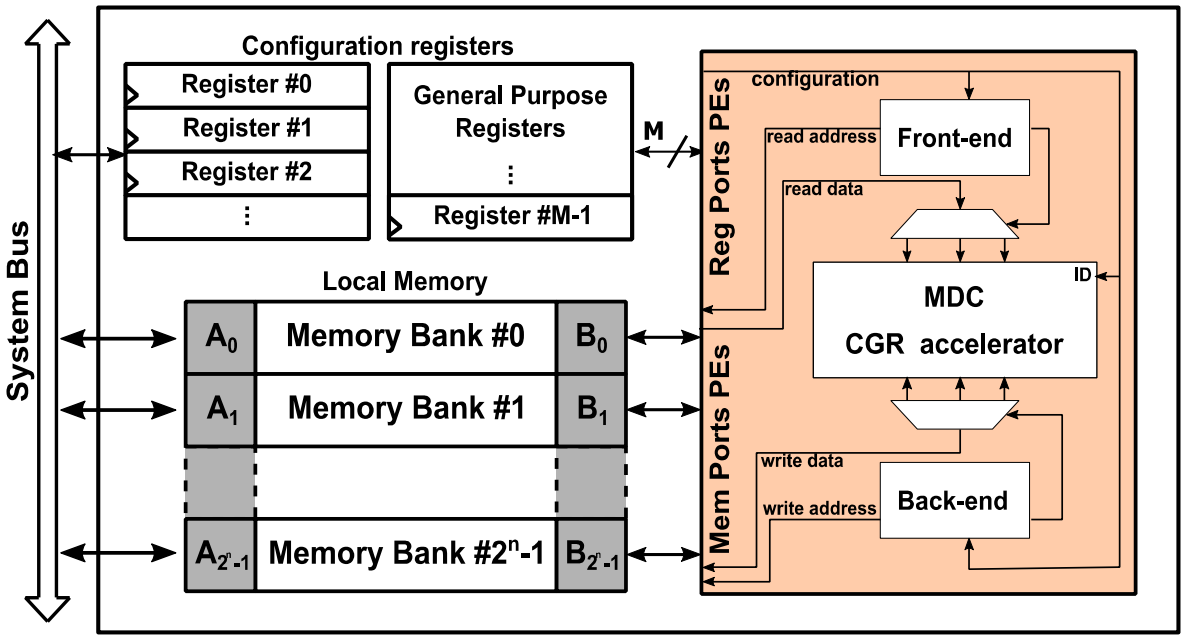


Tutorial Steps

Coprocessor Generation

System Generation

Validation on FPGA



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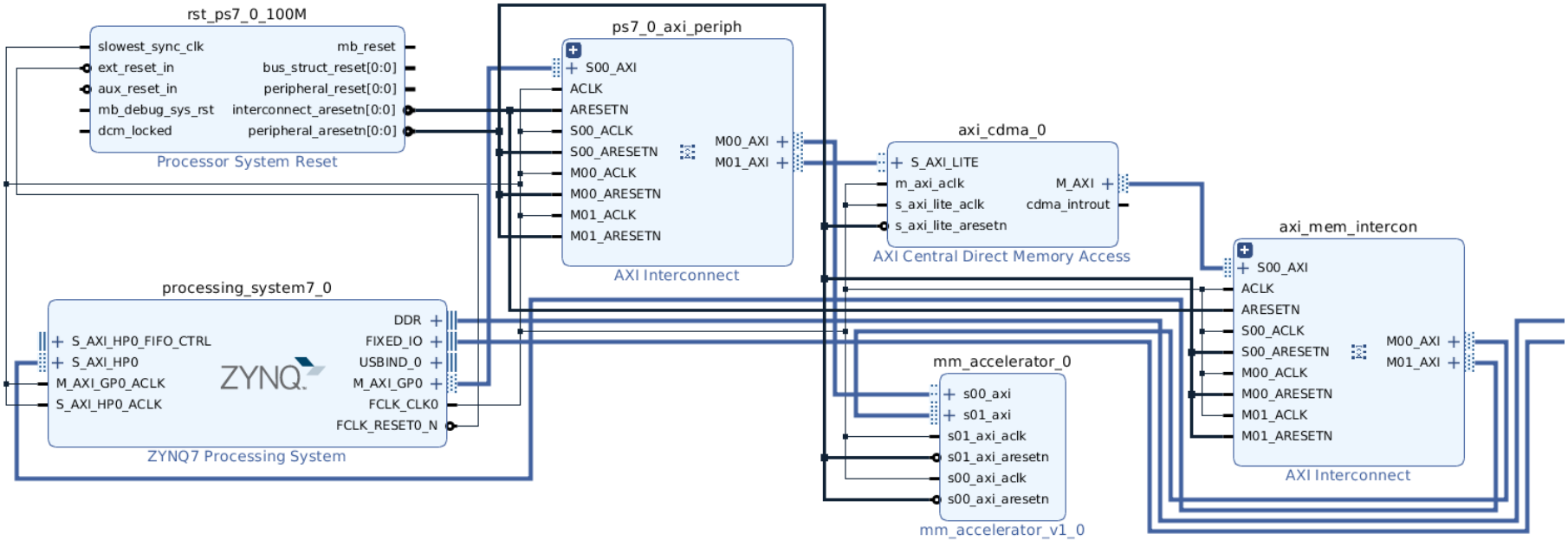

Tutorial Steps

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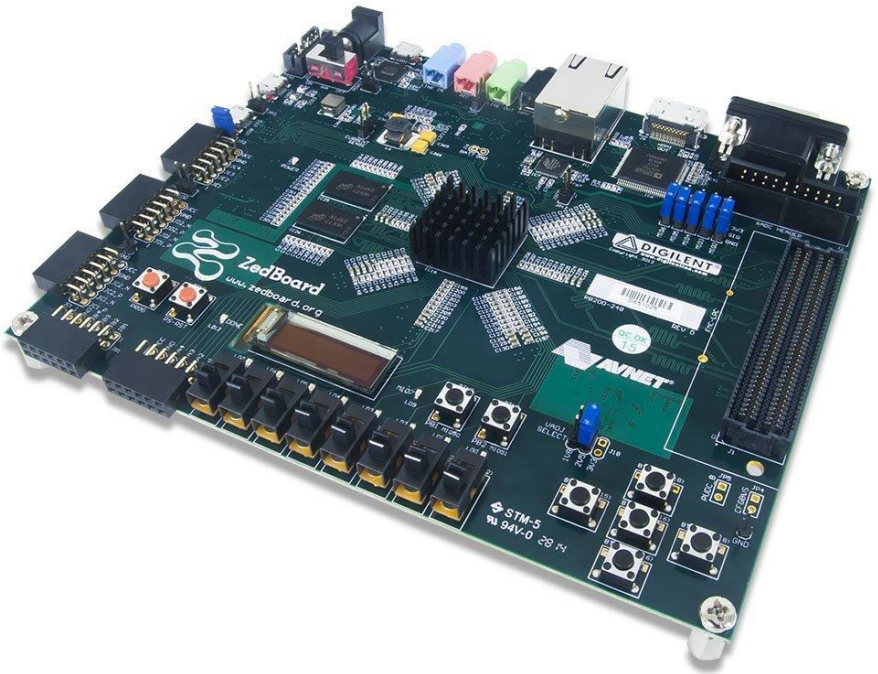

MDC Protocol Generalization

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<protocol>
   <sys_signals>
      <signal id="0" net_port="clock"  is_clock=""…></signal>
      …
   </sys_signals>
   <actor>
      <sys_signals>
         <signal id="0" port="clk" net_port="clock"
…></signal>
         …
      </sys_signals>
      <comm_signals>
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         <signal id="1" port="dout"
channel="data"…></signal>
         <signal id="2" port="wr" channel="en"…></signal>
         …
      <comm_signals>
   </actor>
  <predecessor>
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      <comm_signals>…<comm_signals>
   </predecessor>
   <successor>
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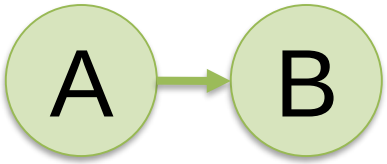
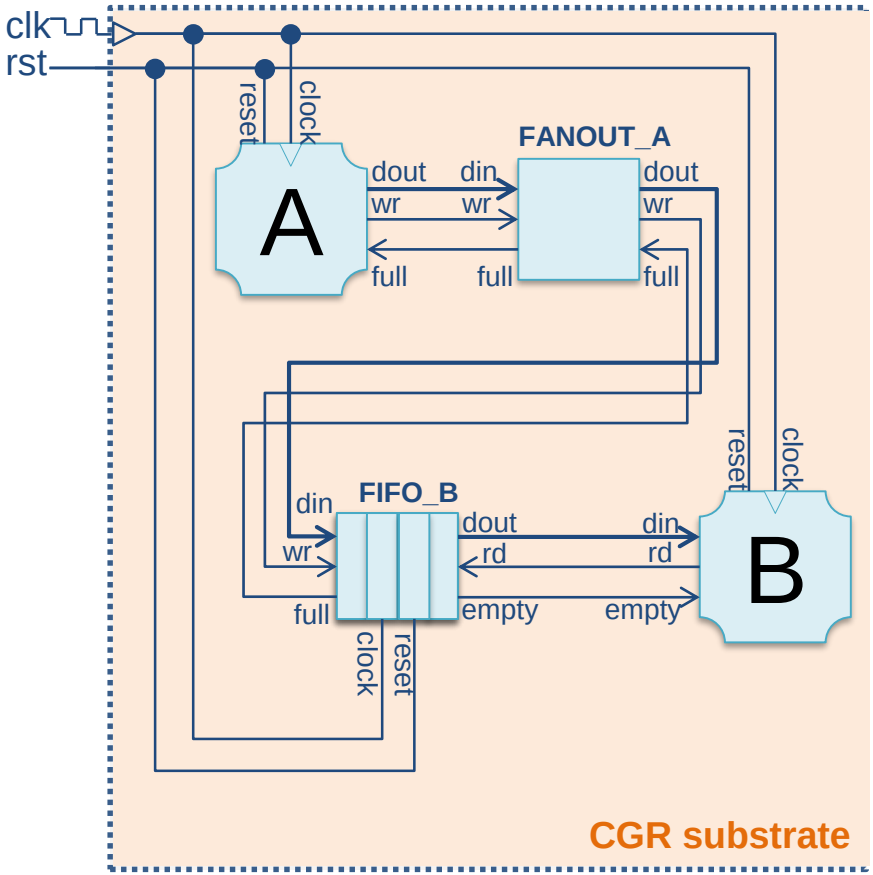
      <comm_signals>…<comm_signals>
   </successor>
</protocol>
```





Tutorial Summary

Coprocessor Generation

MDC Inputs:

files(provided by user)
Dataflow networks
Comm. protocol
HDL comp. libraries

user options
Merging algo
Coupling
Host processor
DMA adoption
Device

System Generation

Vivado Inputs:

files(provided by MDC)
CGR system HDL
High-level drivers
Scripts for Vivado

user options
Simulation
Synthesis

Validation on FPGA

Board Inputs:

files(provided by Vivado)
Bitstream

files(provided by MDC)
High-level drivers

files(provided by user)
Application code

user options
Syst. reconfiguration

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