

<b>Users</b>	<ul style="list-style-type: none"> <li>• Hardware engineers with little experience designing reconfigurable systems.</li> <li>• Hardware engineers targeting regular 2D mesh-type reconfigurable architectures.</li> </ul>
<b>Key Features</b>	<ul style="list-style-type: none"> <li>• Module relocation</li> <li>• Reconfigurable to reconfigurable communications.</li> <li>• Stacking of multiple modules in a clock region.</li> <li>• Hierarchical reconfiguration.</li> <li>• Decouples the static and reconfigurable designs.</li> <li>• Provides LUT-based components for faster reconfiguration</li> <li>• Run-time support for building 2D reconfigurable architectures</li> </ul>
<b>Benefits for the User</b>	<ul style="list-style-type: none"> <li>• Enables the design of complex reconfigurable architectures (i.e., 2D mesh-type reconfigurable architectures) with modules containing LUT-based components.</li> <li>• Enables just-in-time hardware composition.</li> </ul>
<b>Inputs</b>	<ul style="list-style-type: none"> <li>• Static and reconfigurable HDL source files.</li> <li>• Virtual architecture description.</li> <li>• Module interface descriptions (optional).</li> </ul>
<b>Outputs</b>	<ul style="list-style-type: none"> <li>• Static and reconfigurable partial bitstreams.</li> </ul>
<b>Block Design</b>	<p>The diagram illustrates the Block Design process flow. It starts with 'Input file Processing' which receives 'Project file', 'Virtual architecture', and 'Virtual Interfaces'. This leads to two parallel paths: 'Static system generation' and 'Reconfigurable module generation'. Both paths include steps: Netlist Generation, Apply Virtual Architecture, Create Virtual Interface (for static), Apply Virtual Interface, Add Dummy Logic, Placement &amp; Routing, and Bitstream Generation. The static path outputs a 'BIT' file, while the reconfigurable path outputs a 'PBS' file. Both paths also receive 'Static Design Description' (RTL) and 'Reconfigurable Module Description' (RTL) as inputs.</p>
<b>Role in the Toolchain</b>	<ul style="list-style-type: none"> <li>• Enables just-in-time hardware composition by allowing to build regular 2D mesh-type architectures on the fly</li> <li>• Reduces memory footprint in ARTICO<sup>3</sup> partial bitstreams.</li> </ul>