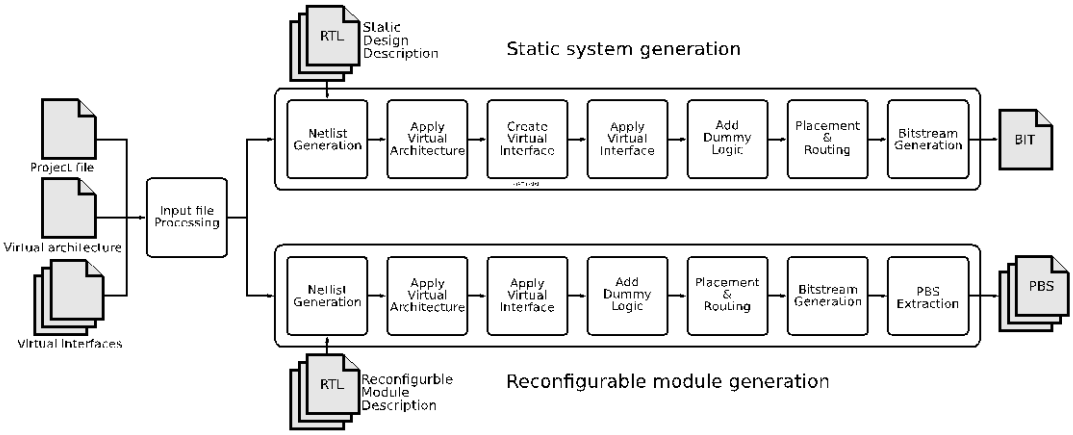
Users	• Hardware engineers with little experience designing reconfigurable systems. • Hardware engineers targeting regular 2D mesh-type reconfigurable architectures.
Key Features	• Module relocation • Reconfigurable to reconfigurable communications. • Stacking of multiple modules in a clock region. • Hierarchical reconfiguration. • Decouples the static and reconfigurable designs. • Provides LUT-based components for faster reconfiguration • Run-time support for building 2D reconfigurable architectures
Benefits for the User	• Enables the design of complex reconfigurable architectures (i.e., 2D mesh-type reconfigurable architectures) with modules containing LUT-based components. • Enables just-in-time hardware composition.
Inputs	• Static and reconfigurable HDL source files. • Virtual architecture description. • Module interface descriptions (optional).
Outputs	• Static and reconfigurable partial bitstreams.
Block Design	
Role in the Toolchain	• Enables just-in-time hardware composition by allowing to build regular 2D mesh-type architectures on the fly • Reduces memory footprint in ARTICo^3 partial bitstreams.