Multi-Dataflow Composer Tool

Dataflow-to-hardware composition and optimization of reconfigurable accelerators

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***Abstract*—UNICA-Eolab and UNISS-IDEA booth is demonstrating the capabilities of the Multi-Dataflow Component tool: a model-based toolset for design and development of virtual coarse-grain reconfigurable circuits providing substrate composition, optimization and integration in real environments.**

***Index Terms*—coarse-grained reconfiguration, virtual reconfiguration, FPGA, ASIC, composition, power-management, DSE, datapath-merging, dataflow**

I. Introduction

Embedded computing systems are pervasive and used in many different application fields such as smart cities, transportation, etc. Complex and distributed infrastructures are required to meet functional and non-functional requirements, associated with dynamic and variable behaviours, real-time constraints and efficient system consumption, which tend to collide. To enable system efficiency, along with optimal energy management, heterogeneous substrates can be used, where reconfigurability can master the required flexibility degree. In particular, Coarse-Grained (CG) virtually reconfigurable accelerators enable supporting several different functionalities, while providing optimal performance. Implementable both in ASIC and on FPGAs, with their modularity they allow deep customization and optimization of the involved elements. Nevertheless, they are affected by Design, Debug and Mapping issues. Custom hardware designs imply to describe the micro-architecture at the RTL level; application details have to be known, requiring effort in coding and debugging. Moreover, dimensioning the underlying structure and mapping multi-modal/multi-functional applications over it are challenging.

II. The Multi-Dataflow Composer

The Multi-Dataflow Composer (MDC) tool is a software framework for automatic generation and management of CG reconfigurable systems, based on the dataflow model of computation. Its components, depicted in Figure 1, are:

1) Baseline Core - performing dataflow-to-hardware composition, by means of datapath merging techniques [1]. Kernels are provided as dataflow networks, and target agnostic RTL description is derived. [FPGA/ASIC]
2) Structural Profiler - exploring the design space of the implementable multi-functional systems. Optimal substrate is chosen on the basis of the given frequency and area constraints [1]. [ASIC]
3) Dynamic Power Manager - performing model-level logic partitioning of the substrate to determine optimal power/clock domains, and apply saving strategies [2], [3]. [FPGA/ASIC]
4) Co-Processor Generator - customizing a Xilinx-compliant multi-functional IP with its APIs. [FPGA]

MDC has been already successfully adopted in different applications fields, like multi-media coding [1] and neural signal decoding [4]. Videos and tutorials can be found at [5].

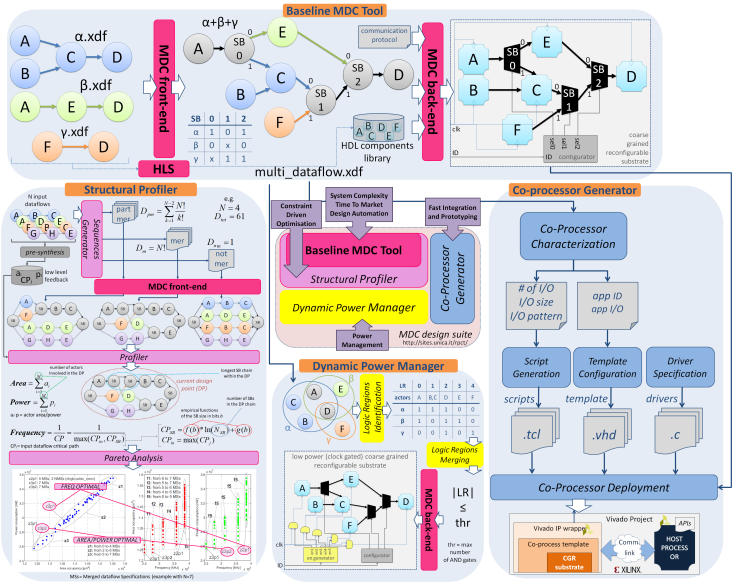

Fig. 1. MDC tool and its extension.

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