

CPS-School 2018
Alghero – 21 September 2018



Tiziana Fanni¹, Alfonso Rodríguez²

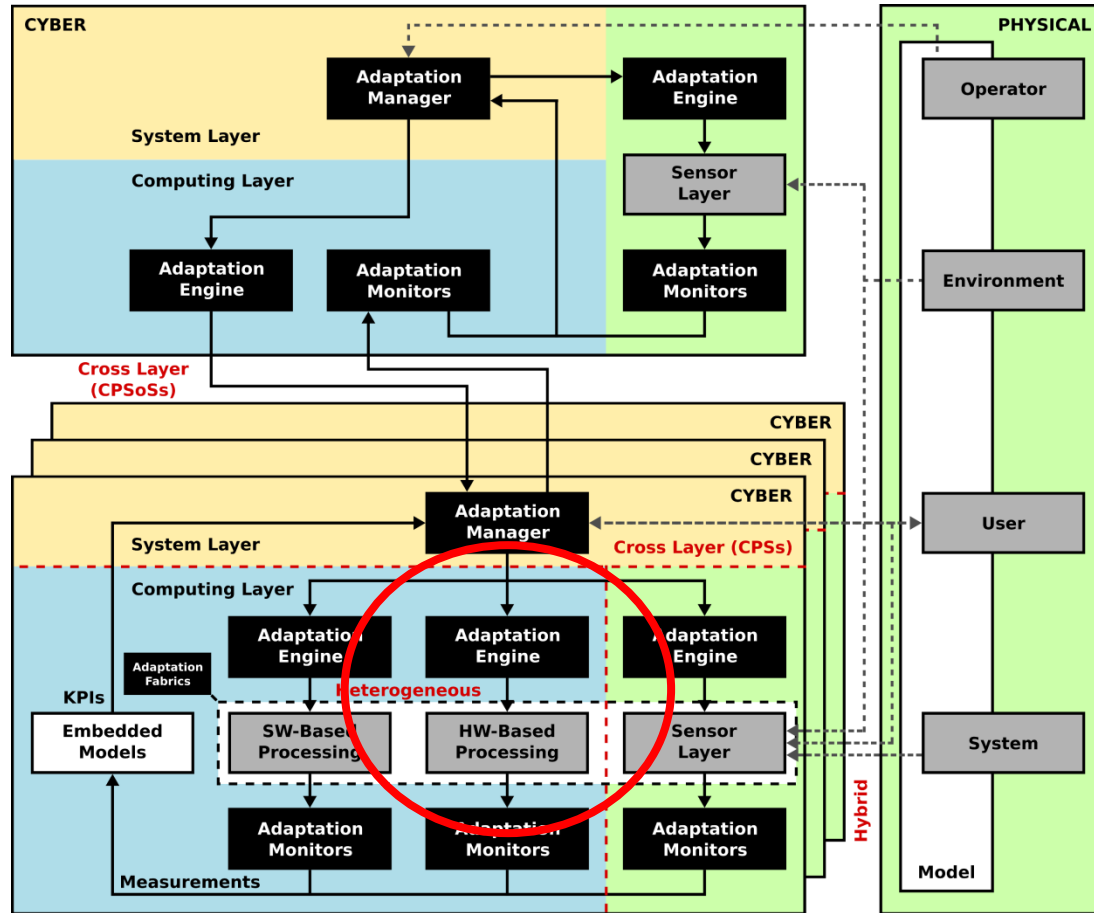
¹Università degli Studi di Cagliari, ²Universidad Politécnica de Madrid

Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems



Horizon 2020
European Union funding
for Research & Innovation

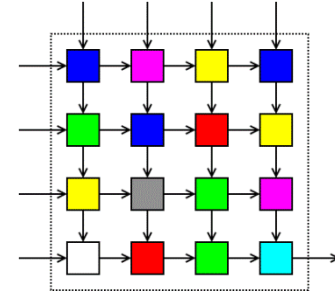
Self-Adaptation in CERBERO H2020



DPR & CG-VRC

DPR → Dynamic and Partial Reconfiguration

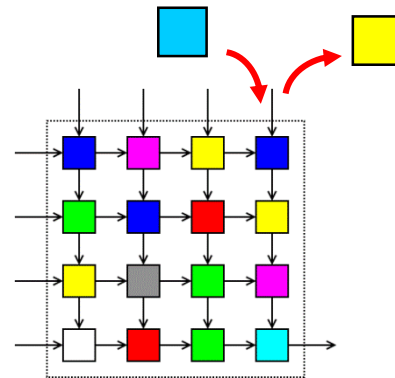
- Lower reconfiguration speeds
- Better operation speed (no mux/less logic)
- Better Resource Utilization (no dark logic)
- Higher Flexibility and Scalability
- Technology dependent (FPGA)



DPR & CG-VRC

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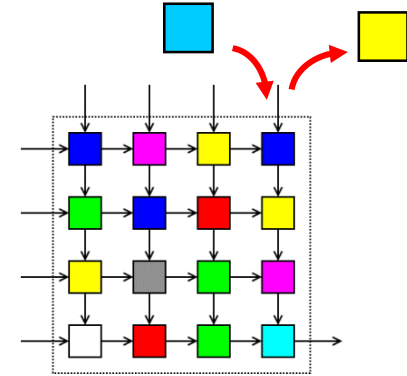
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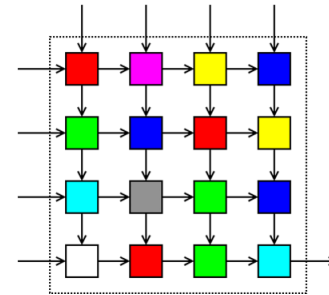
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CG-VRC → *Coarse Grain - Virtual Reconfigurable Circuits*

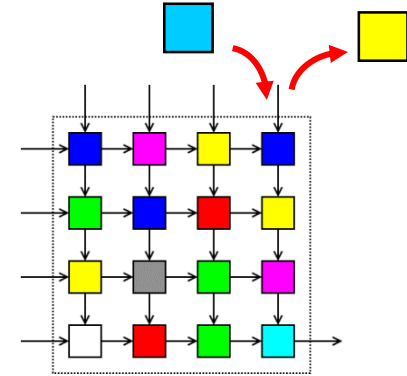
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- Technology independent (ASIC or FPGA)



DPR & CG-VRC

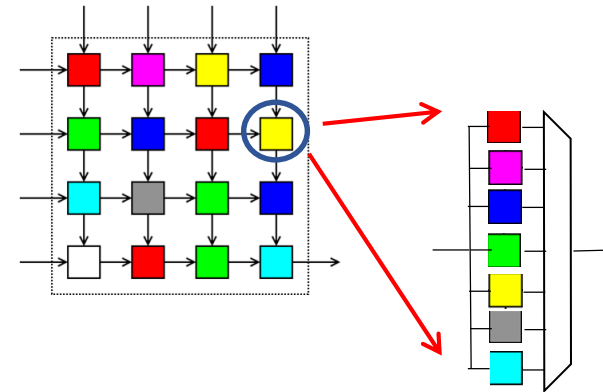
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MDC Tool: Dataflow to HW Mapping

**Multi Dataflow
Composer Tool**

Structural Profiler

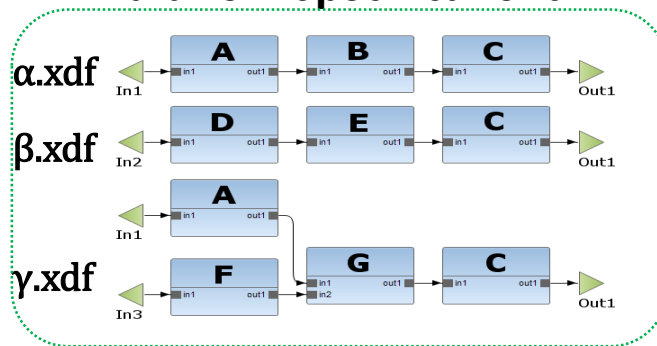
Power Manager

*Co-Processor
Generator*

MDC design suite

<http://sites.unica.it/rpct/>

Dataflow Specifications



MDC Tool: Dataflow to HW Mapping

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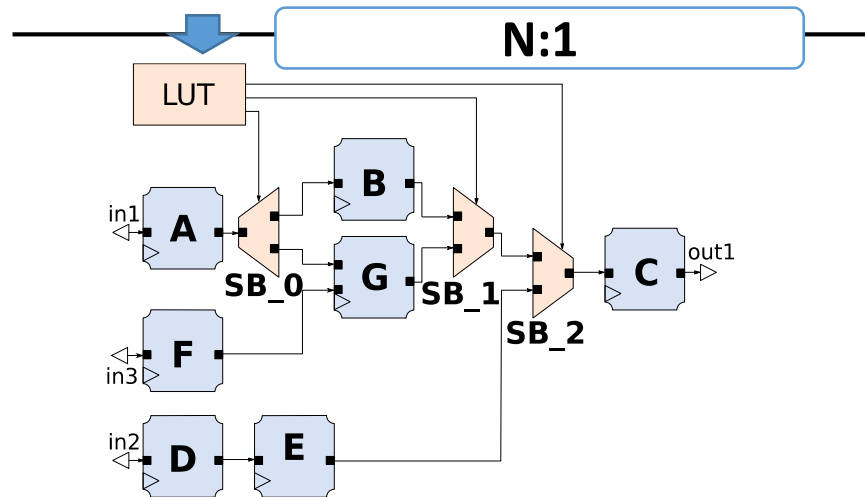
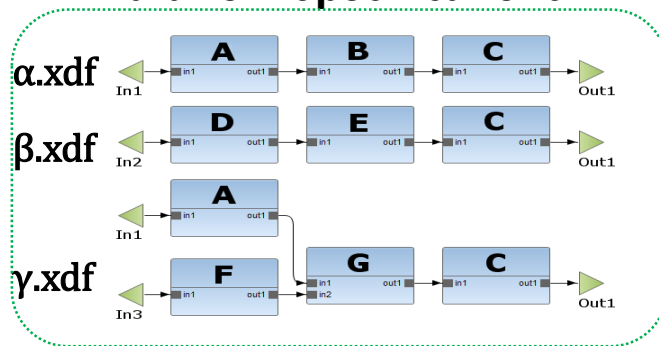
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Dataflow Specifications



MDC Tool: Coprocessor Generator

Co-Processor Generator:

generation of ready-to-use Xilinx IPs

**Multi Dataflow
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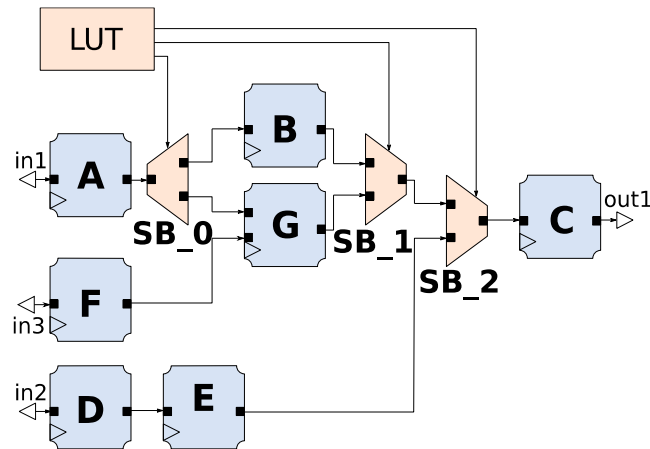
Structural Profiler

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MDC Tool: Coprocessor Generator

Co-Processor Generator:

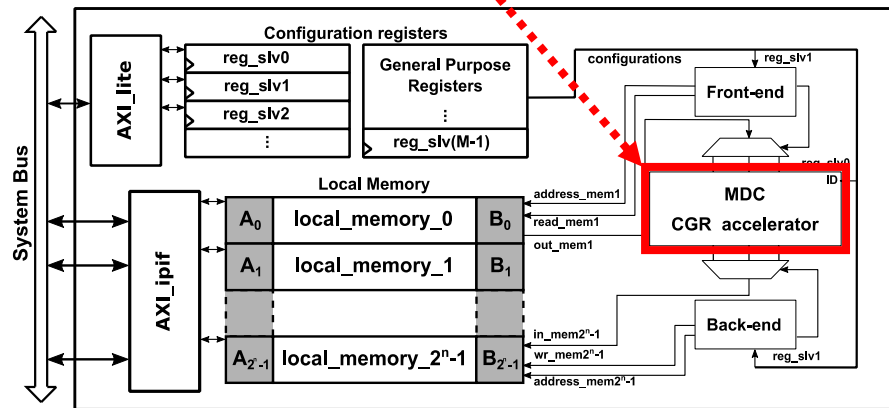
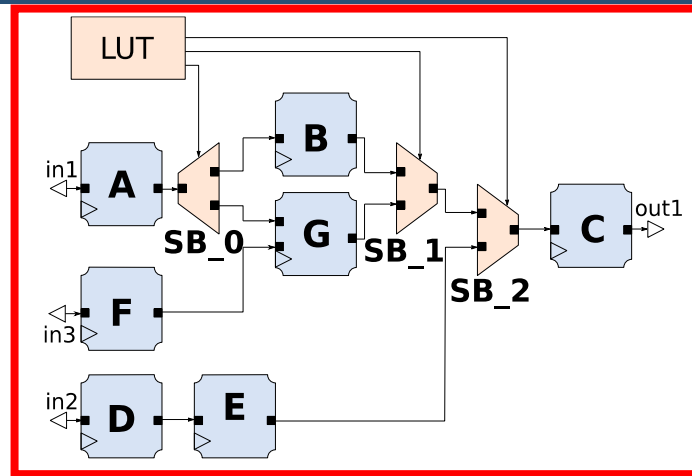
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**Multi Dataflow
Composer Tool**
Structural Profiler
Power Manager

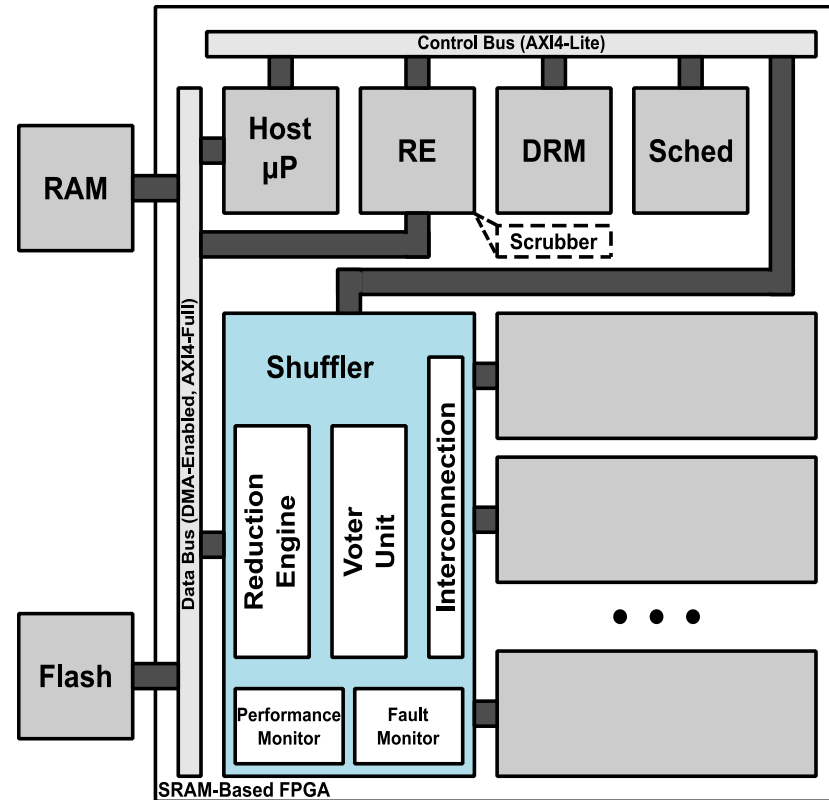
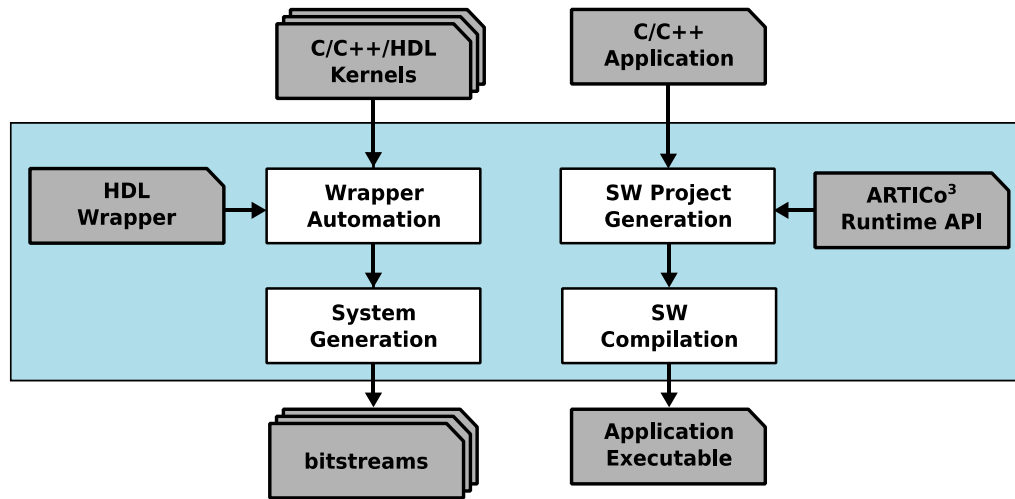
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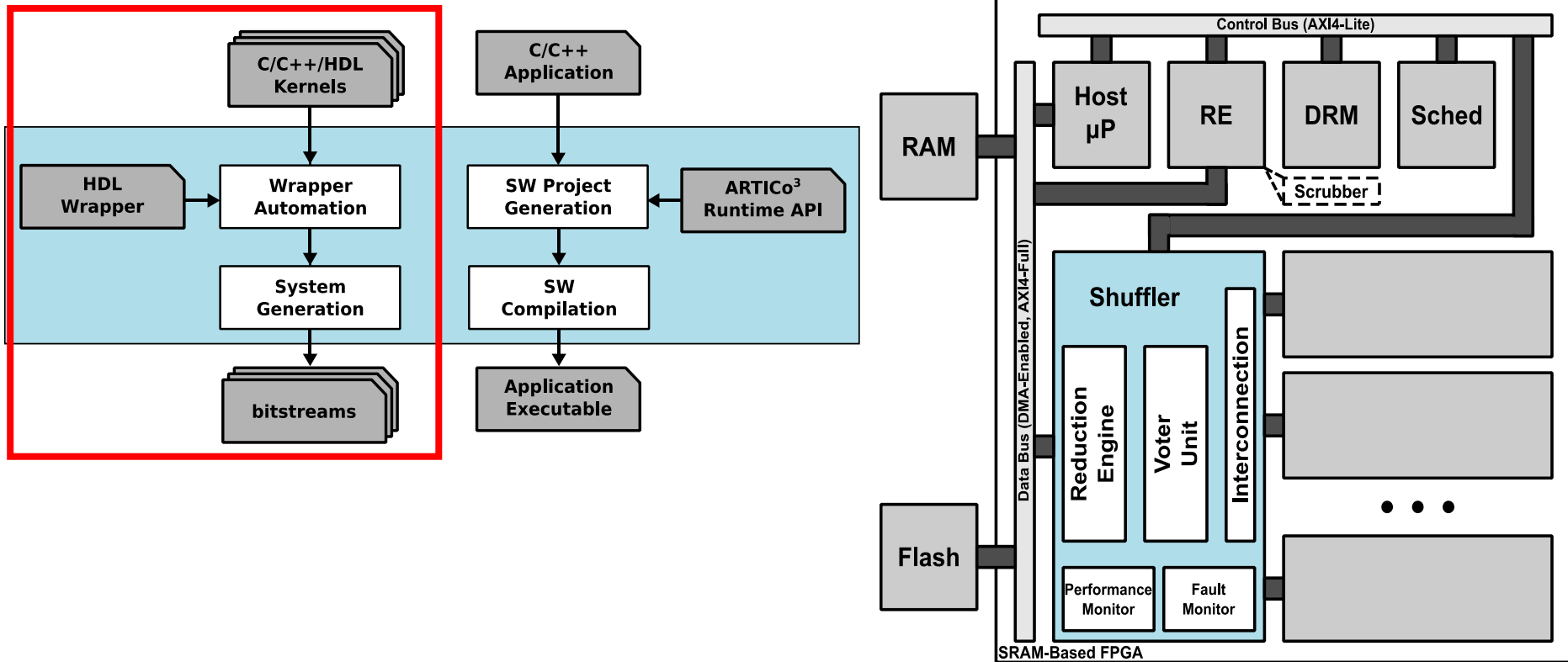
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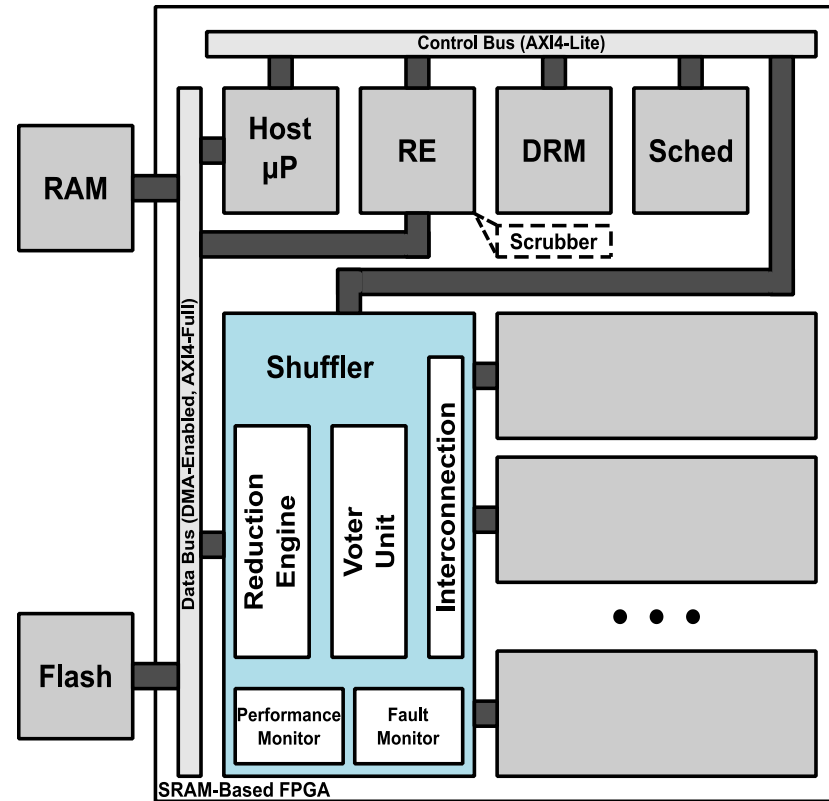
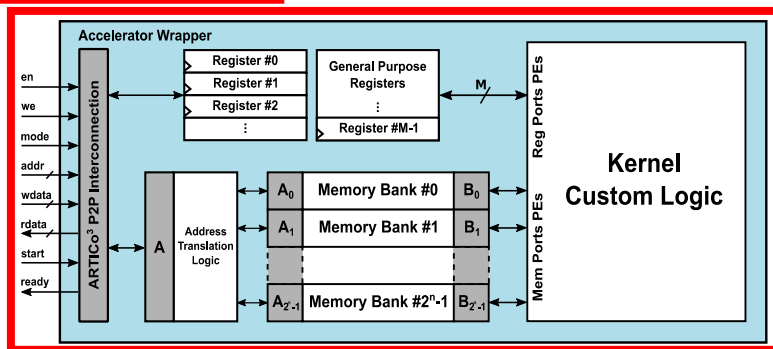
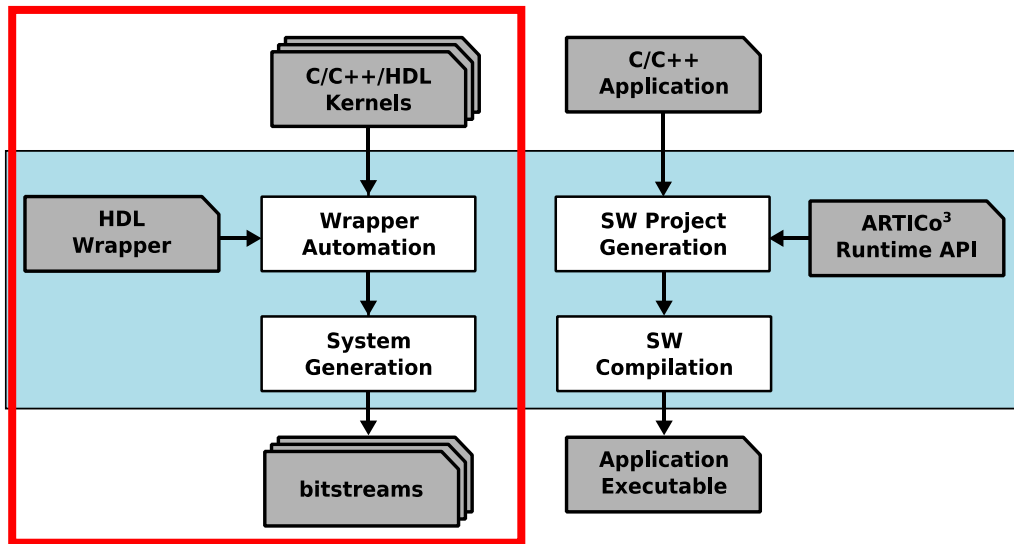
ARTICo³ Framework



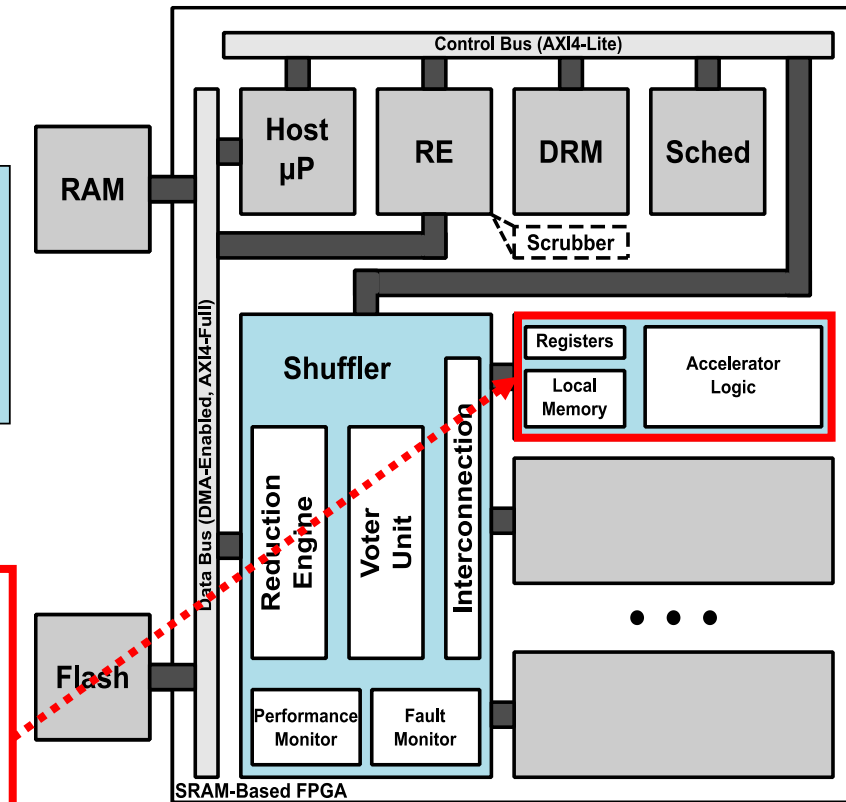
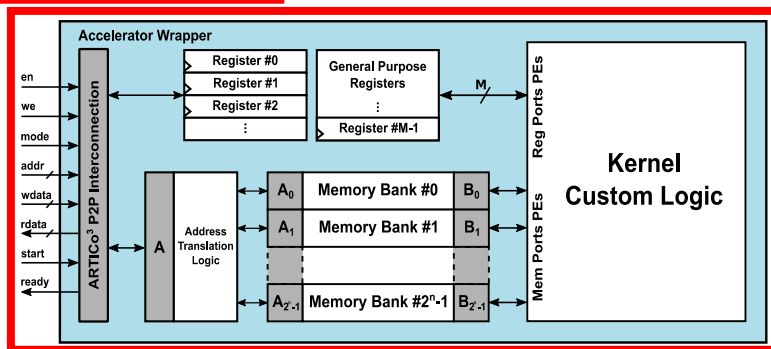
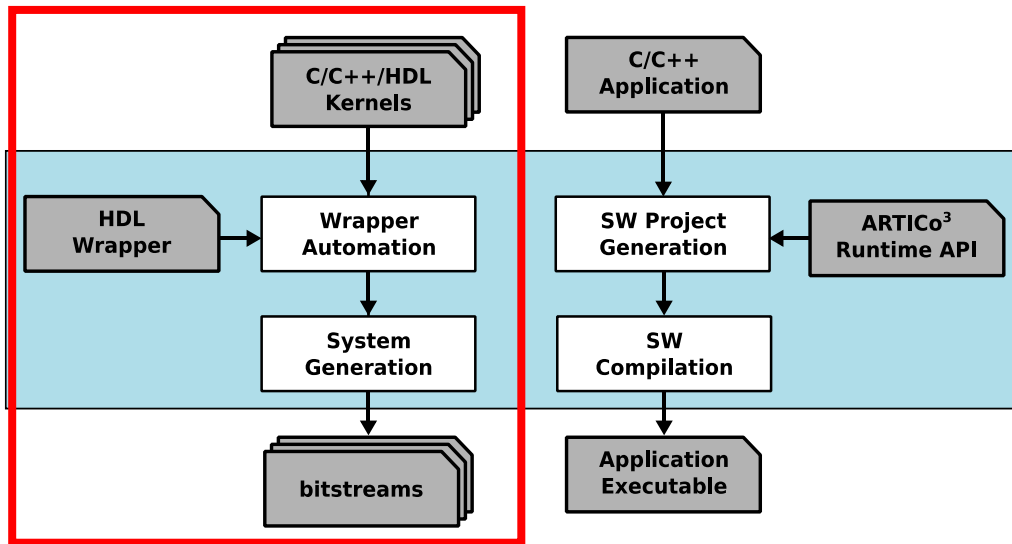
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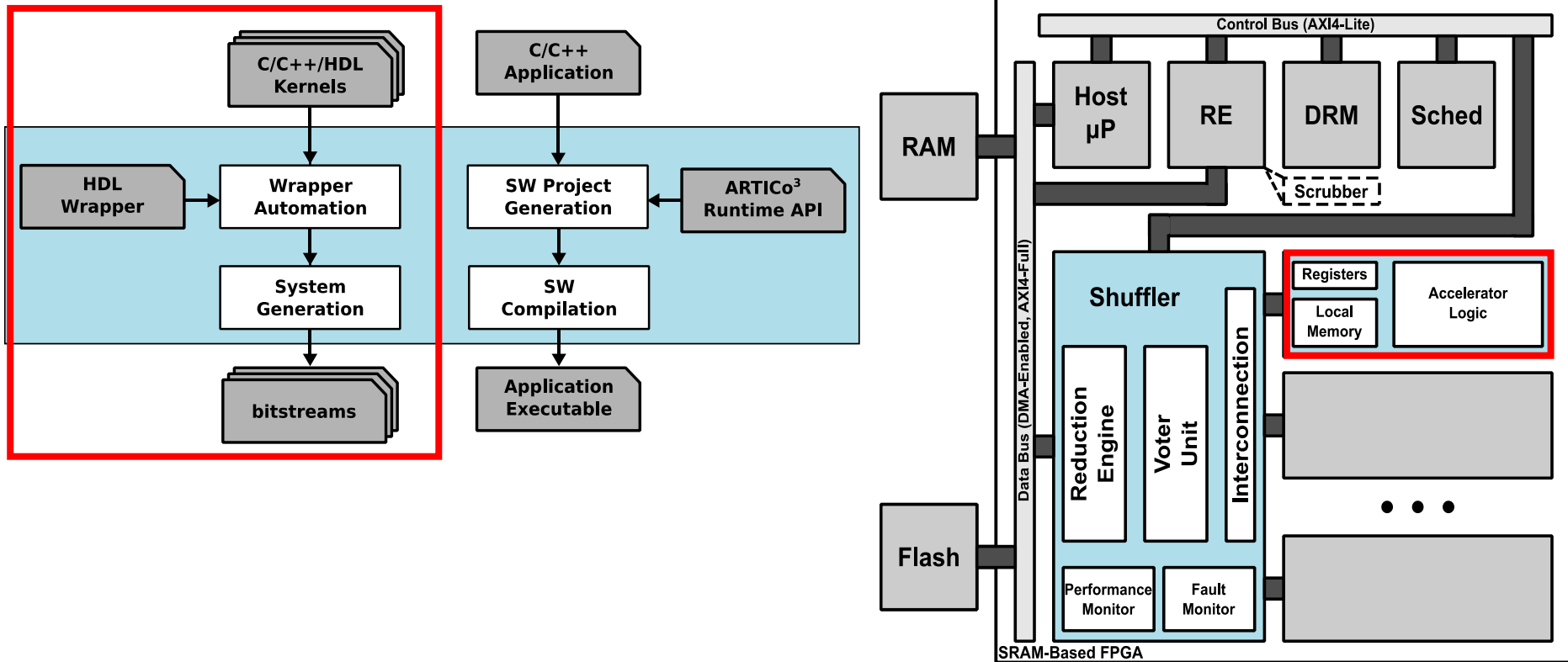
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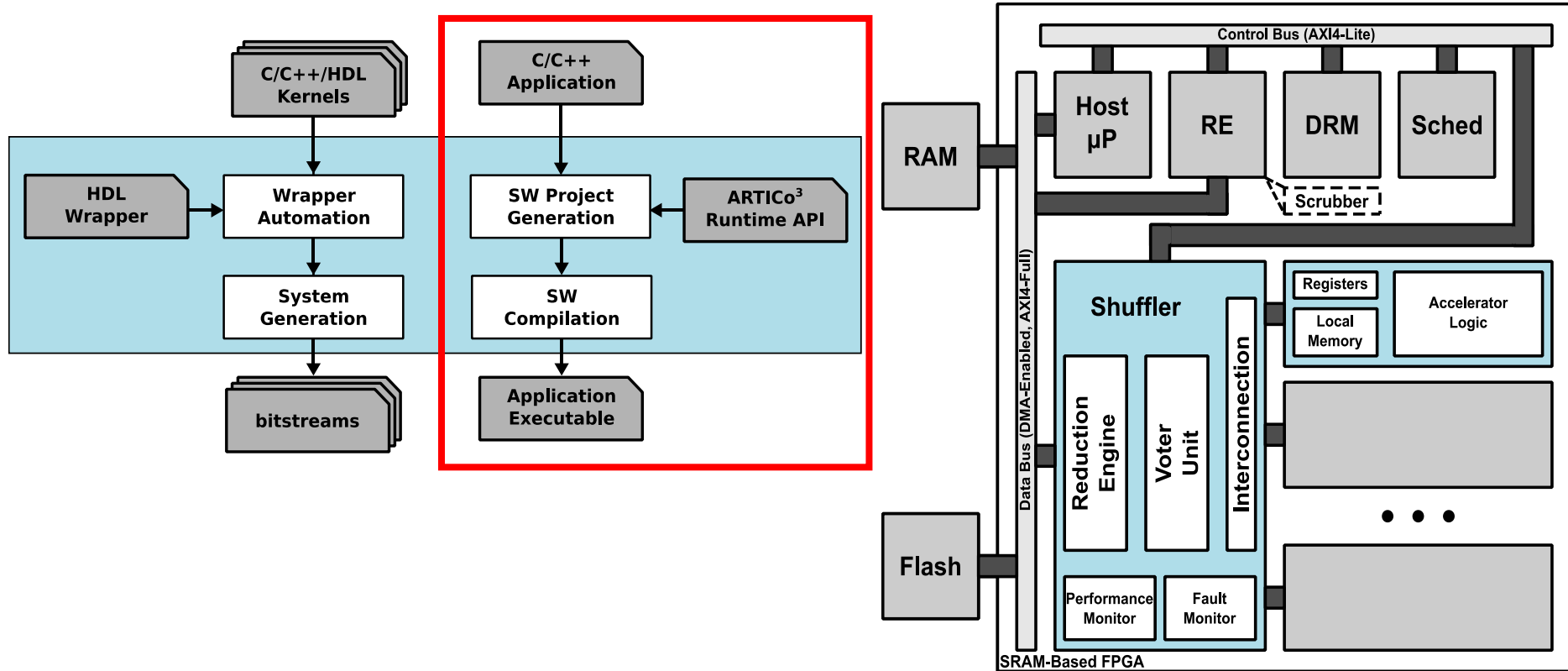
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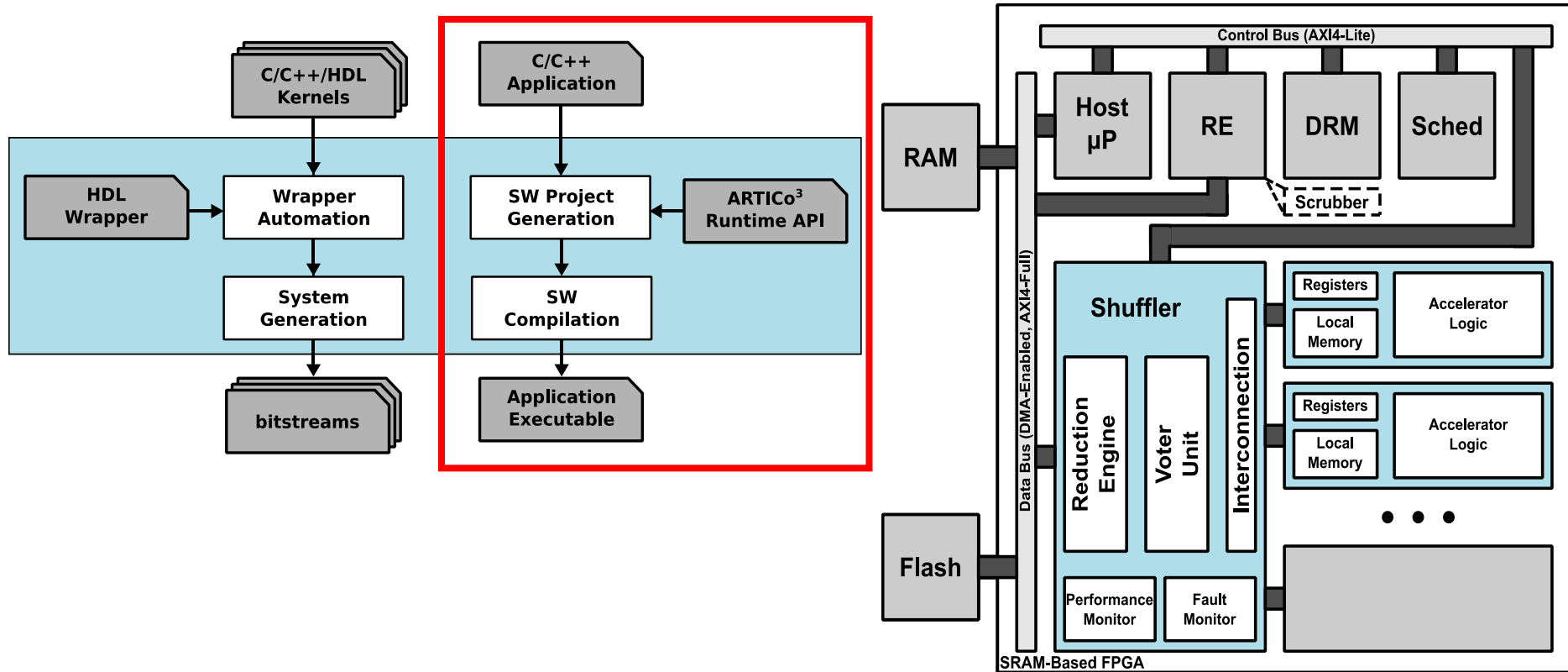
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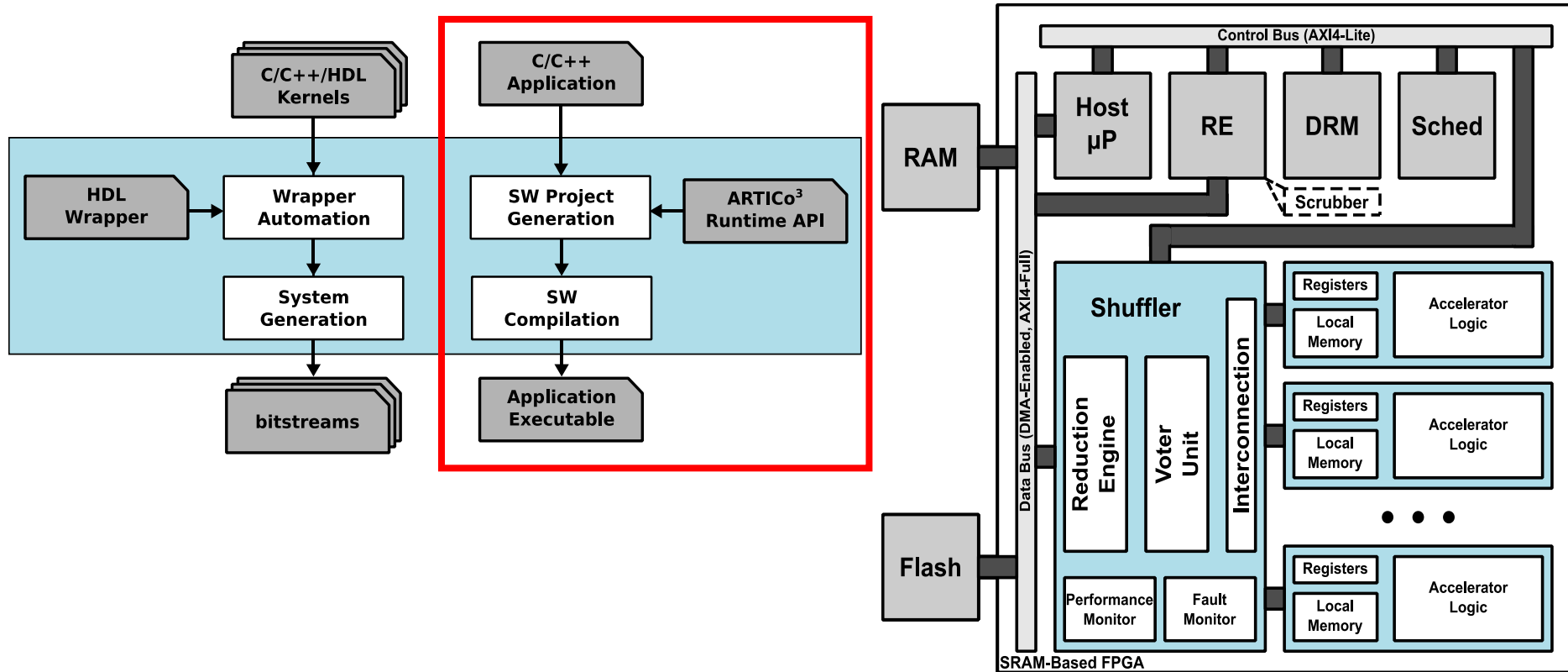
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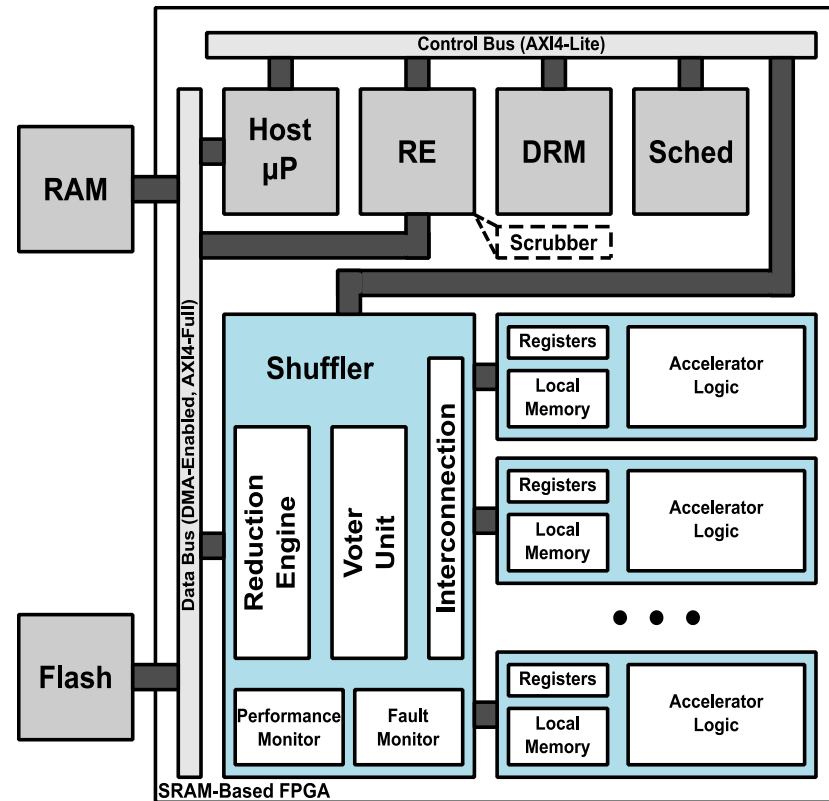
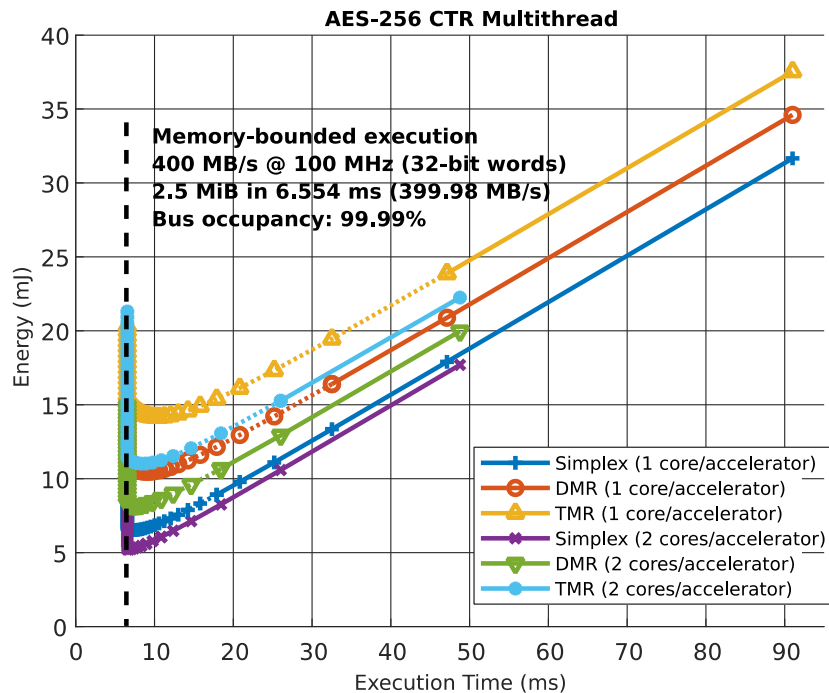
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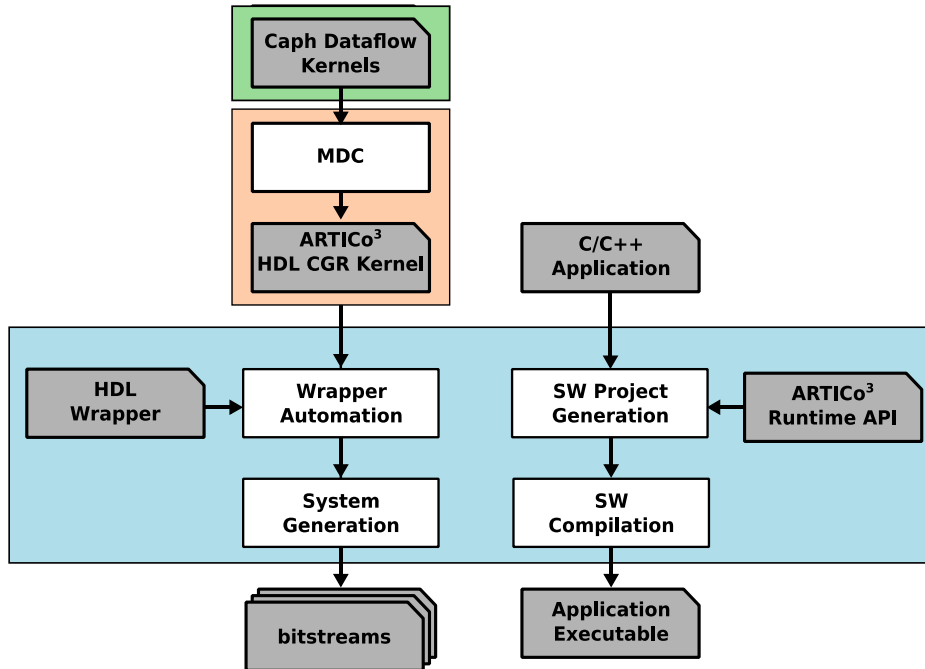
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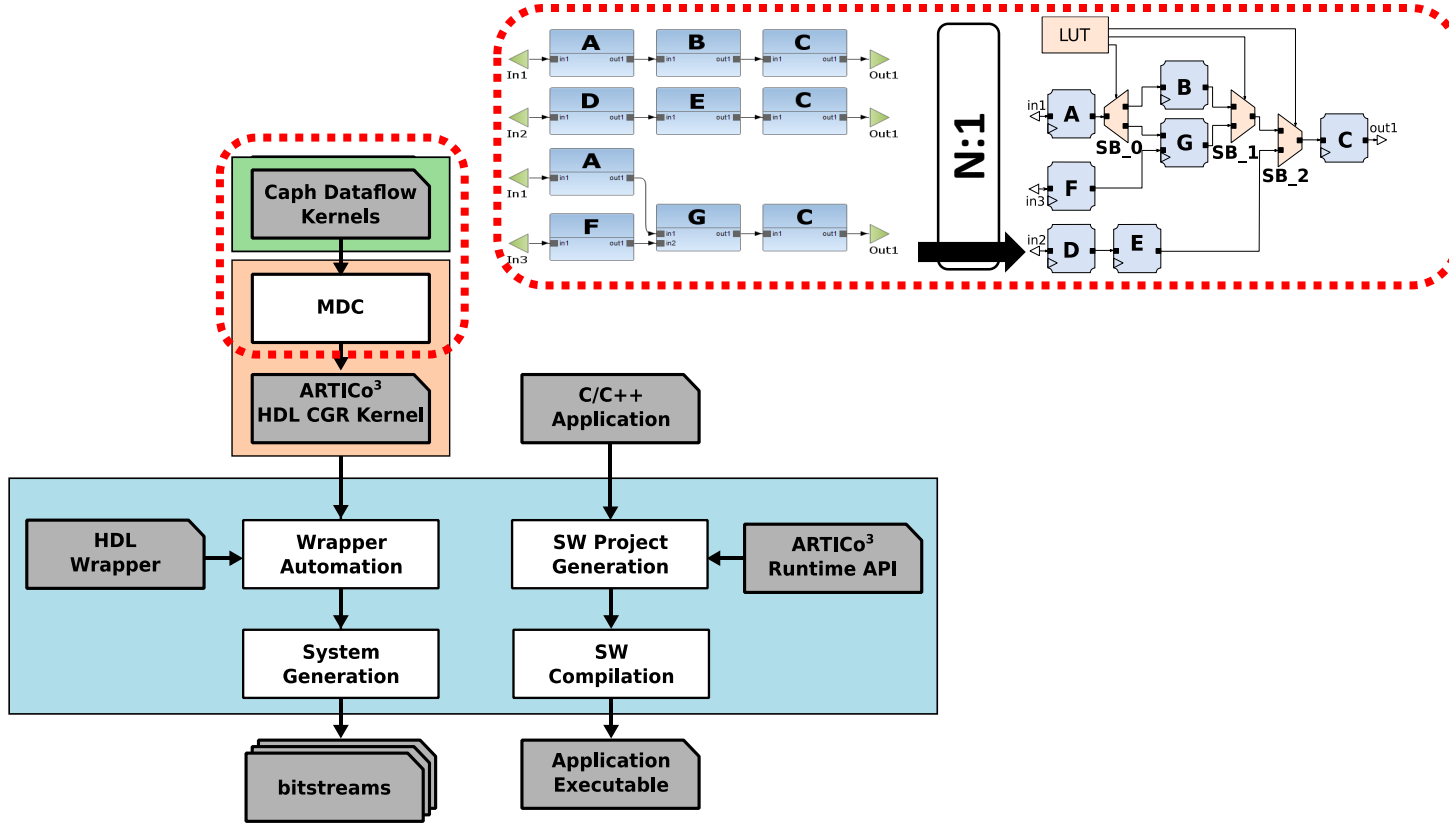
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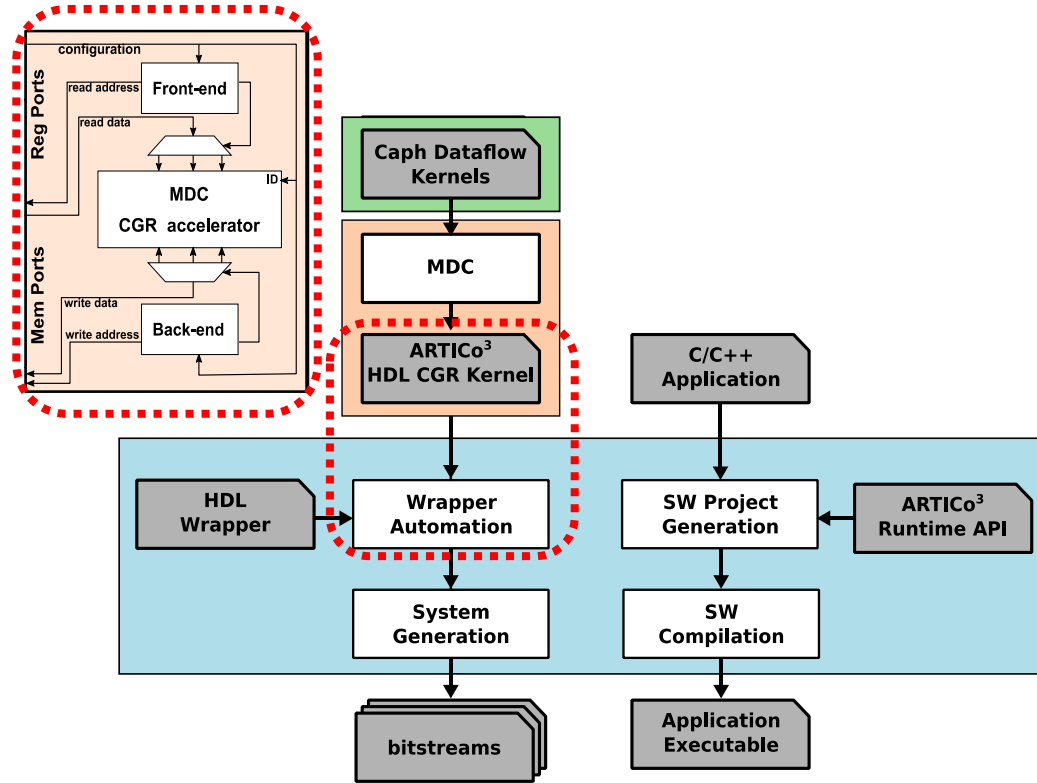
Multi-Grain Adaptivity



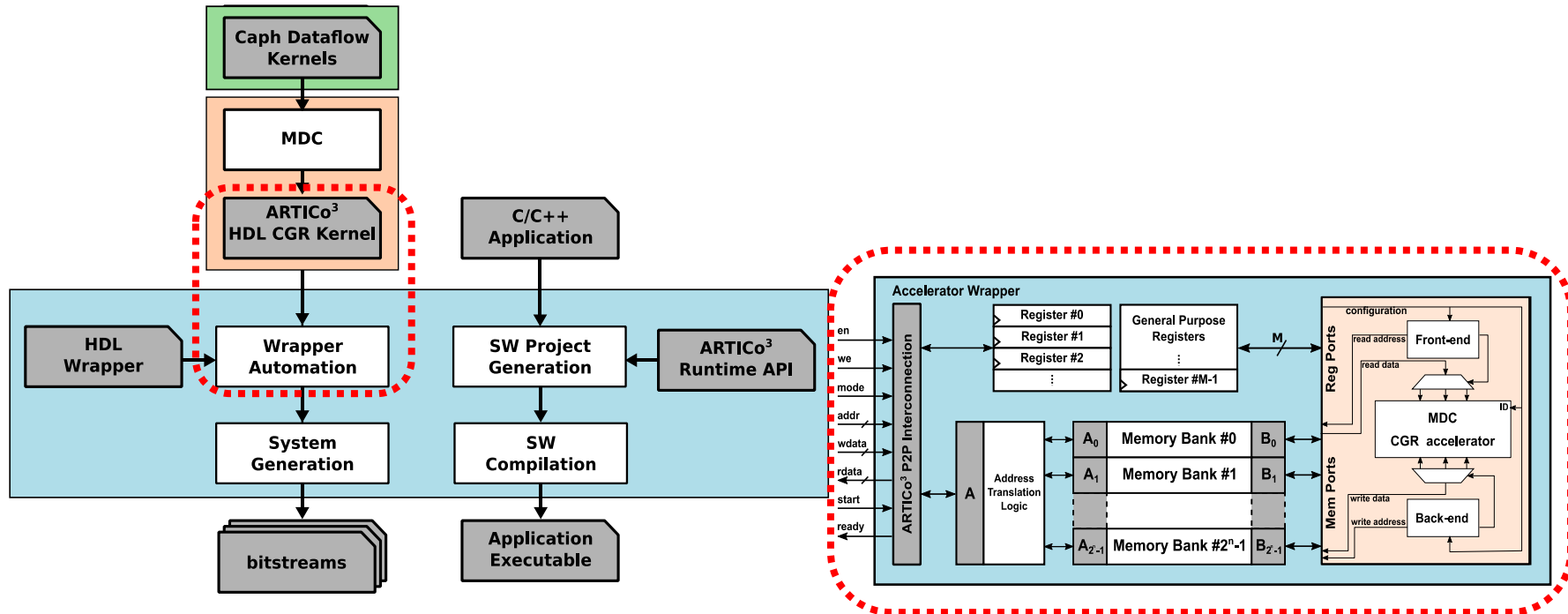
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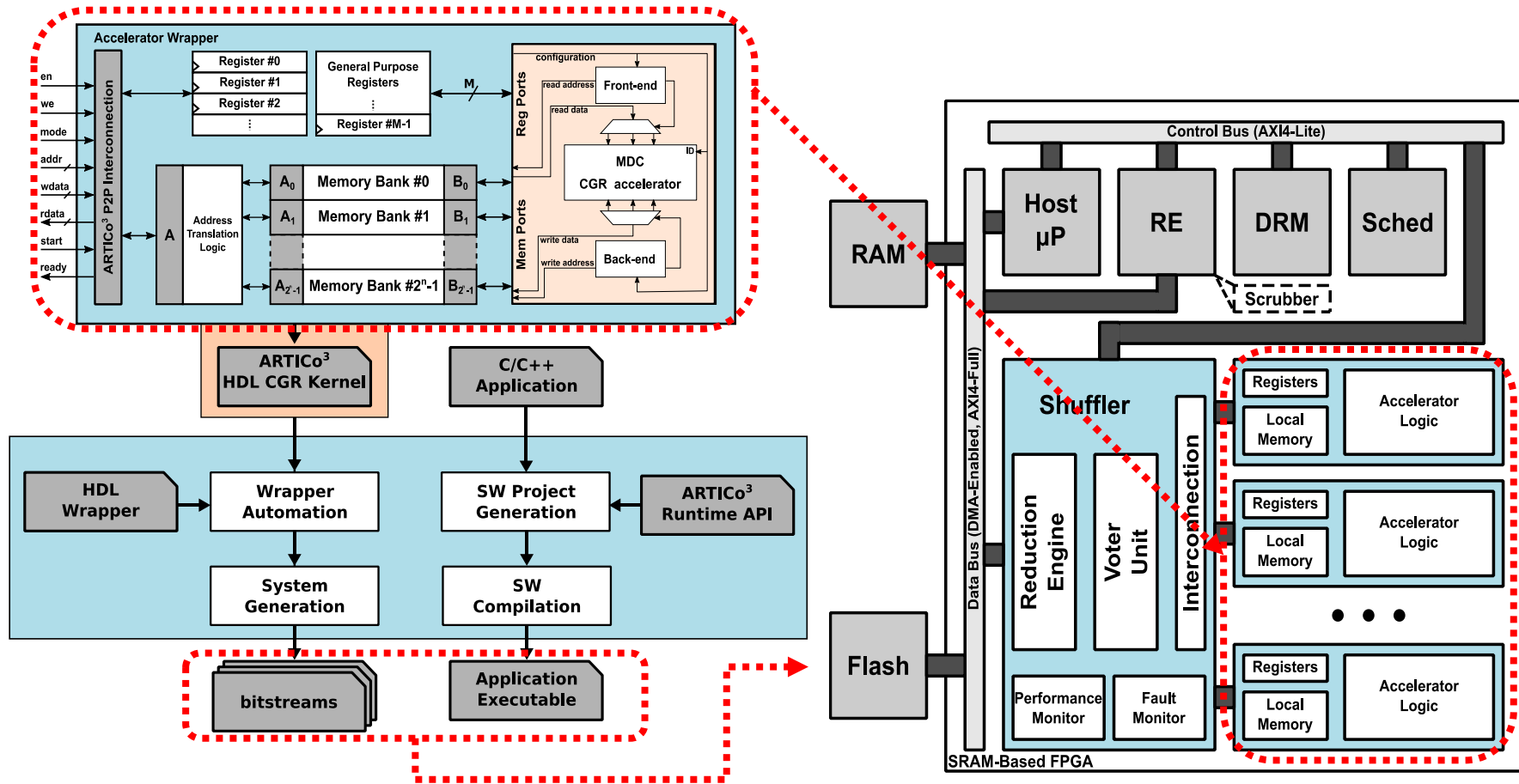
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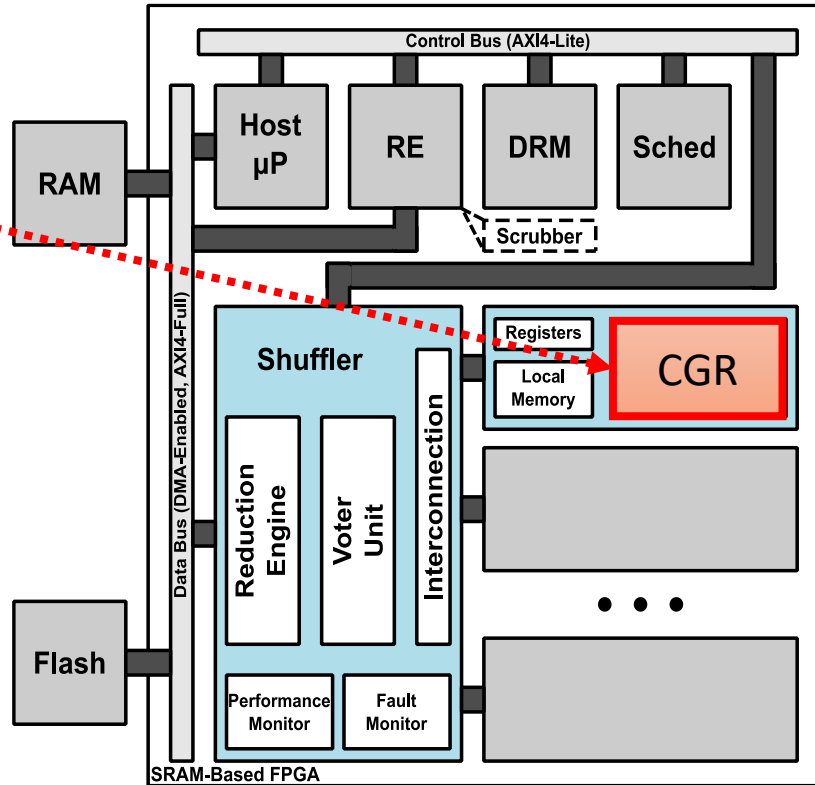
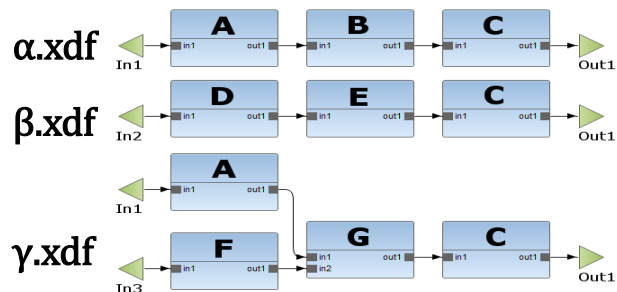
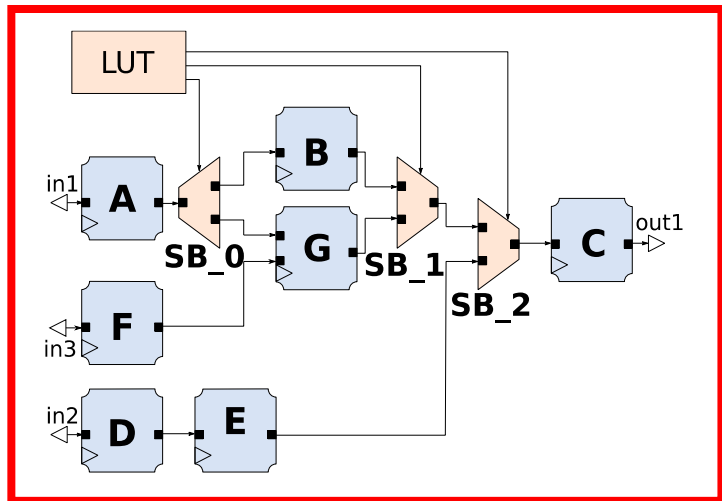
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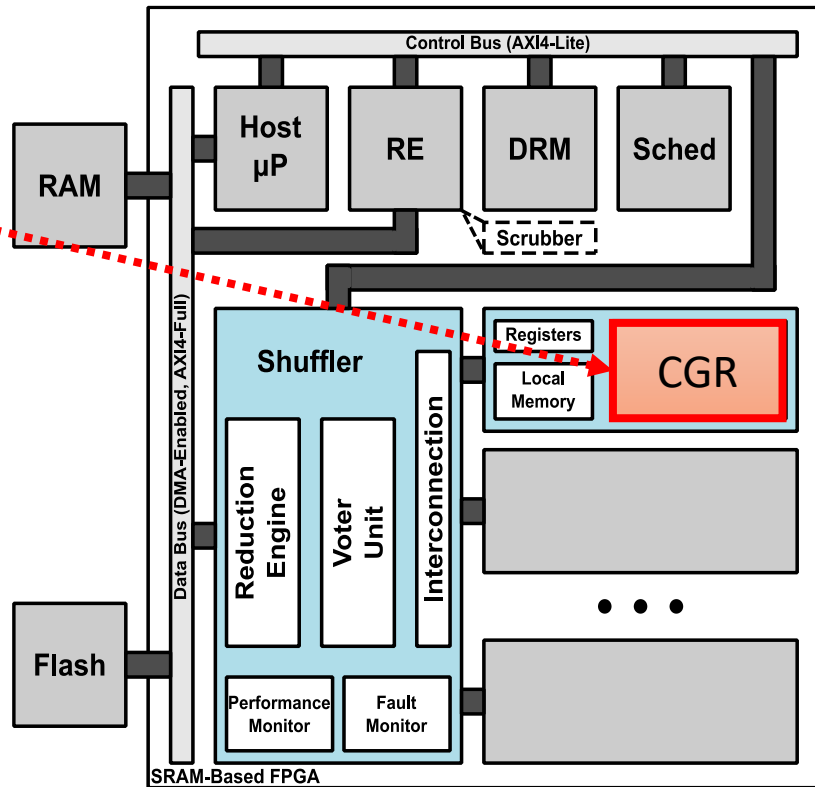
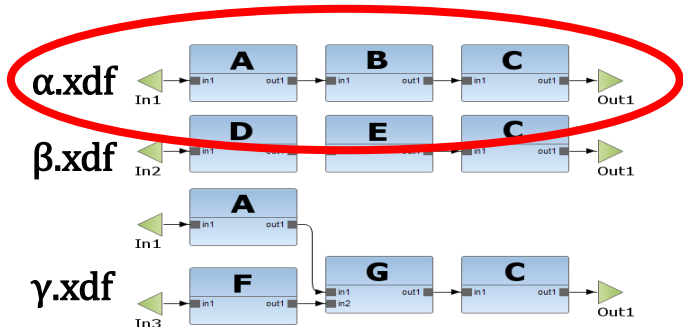
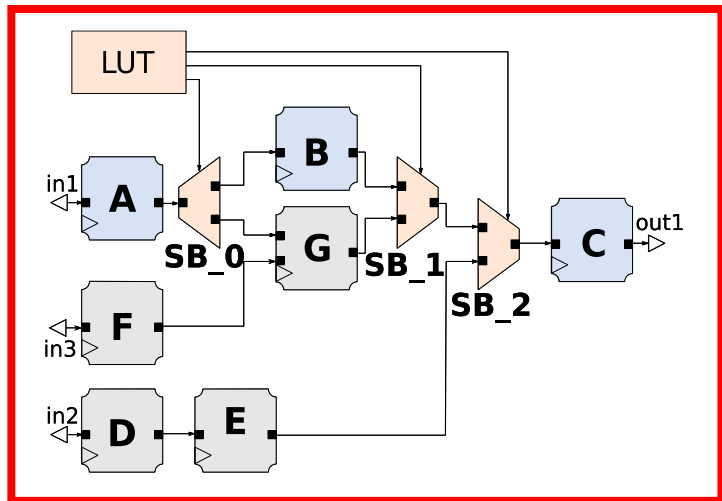
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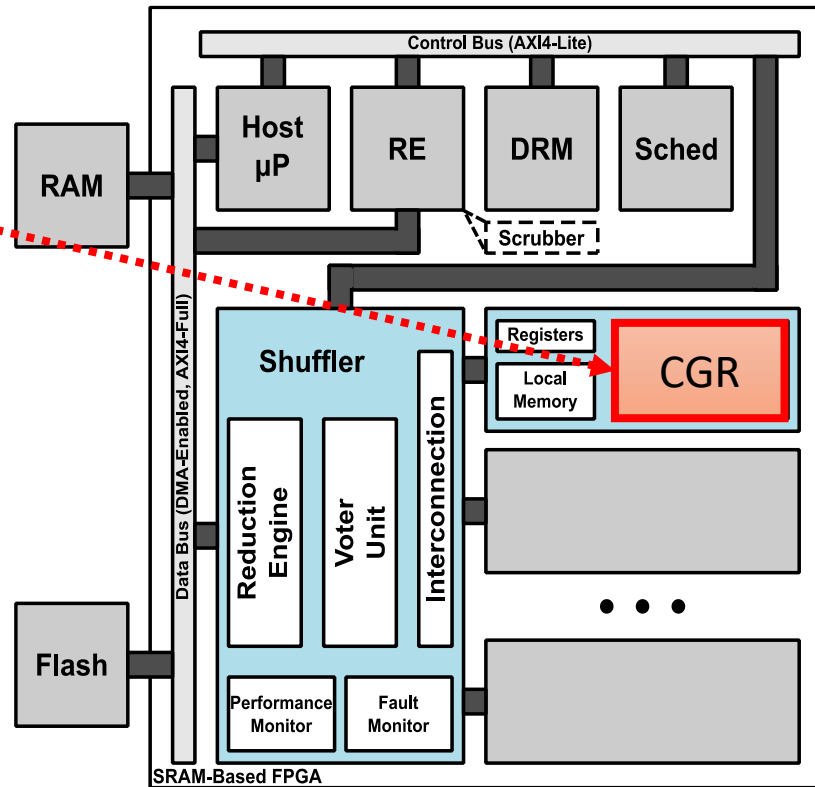
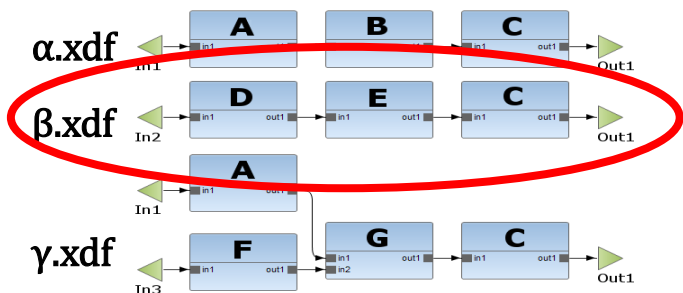
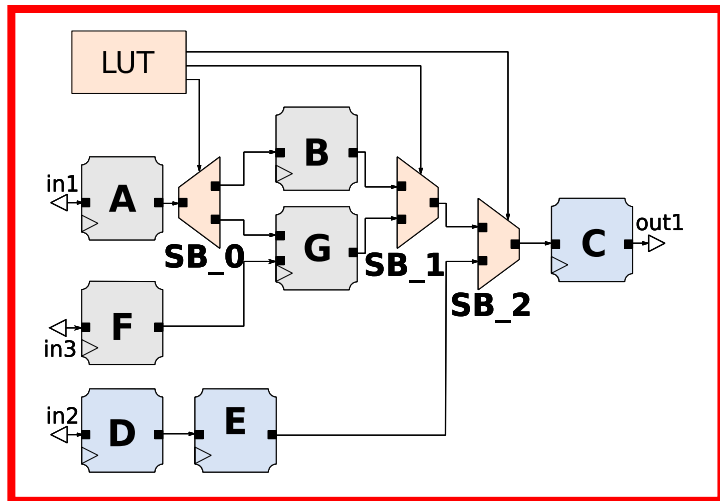
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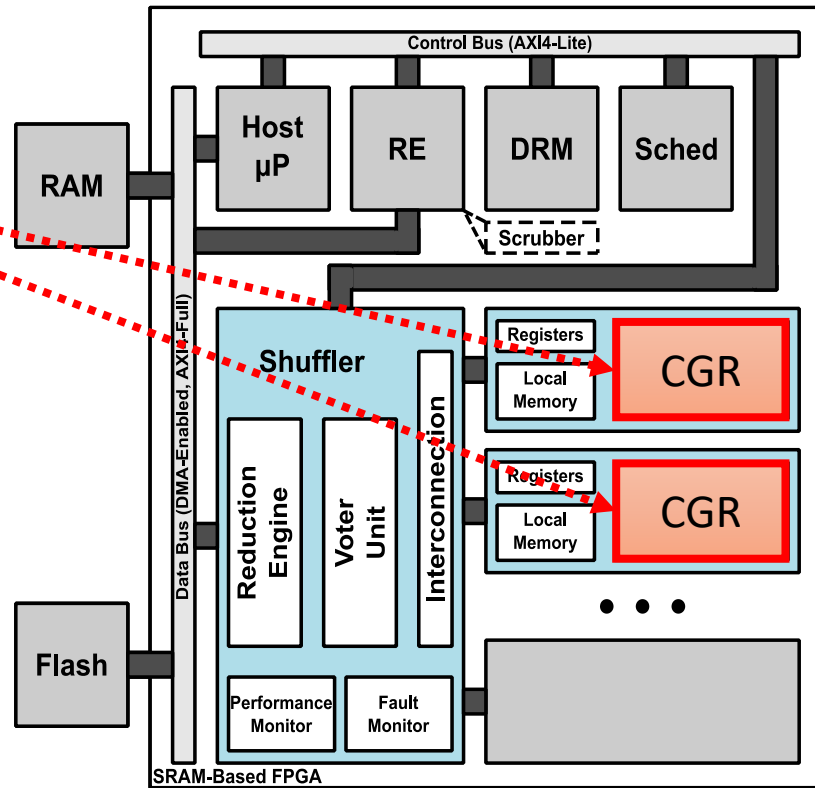
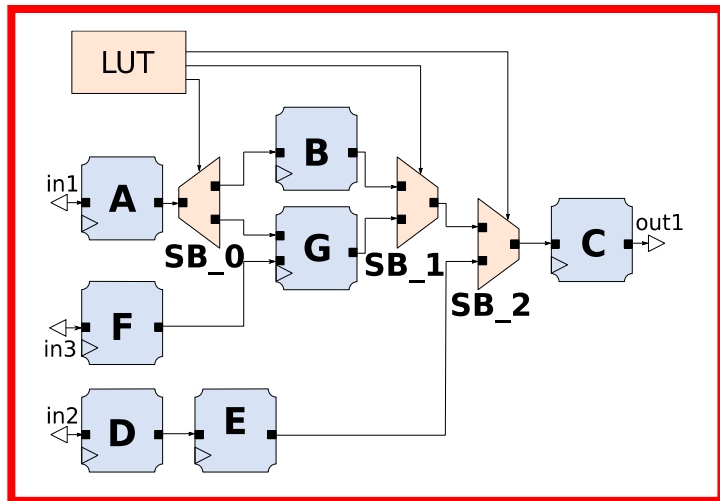
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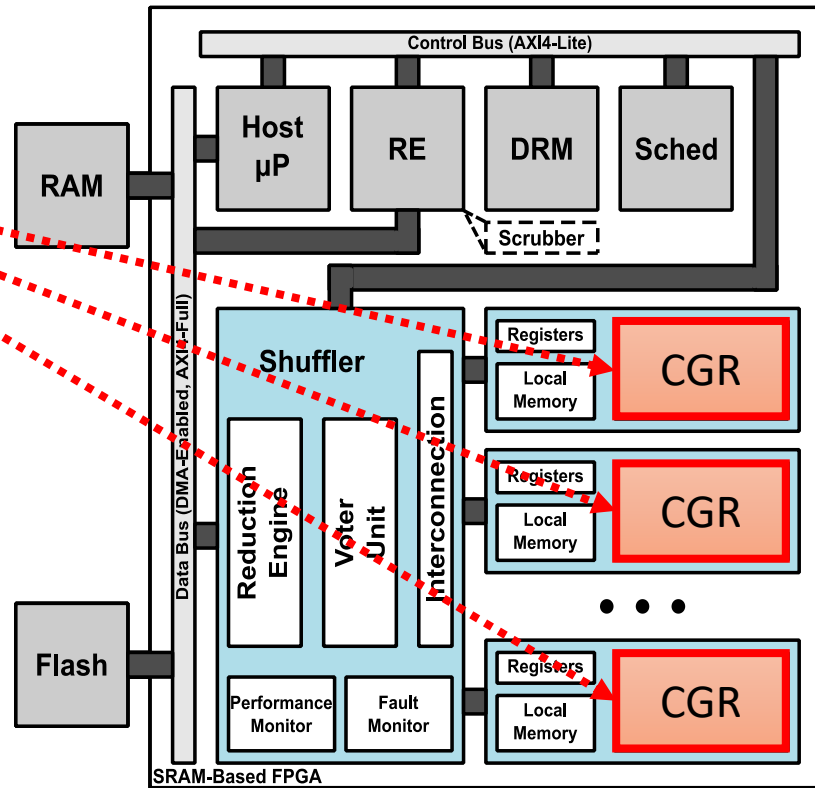
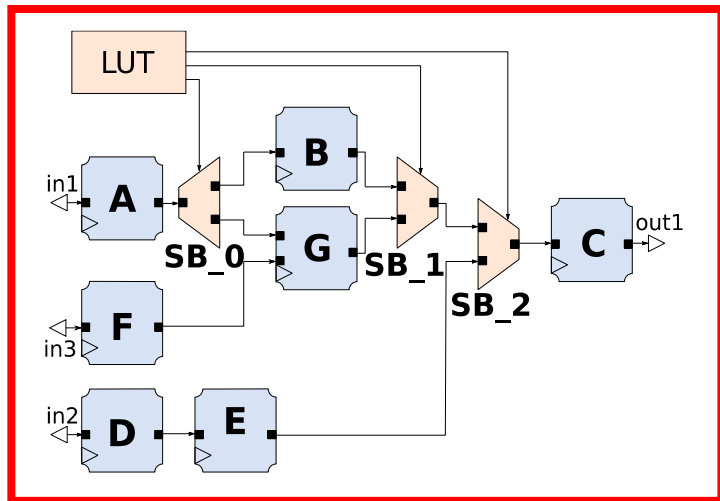
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Multi-Grain Adaptivity



Multi-Grain Adaptivity



Experimental Results – Reconfiguration Overhead

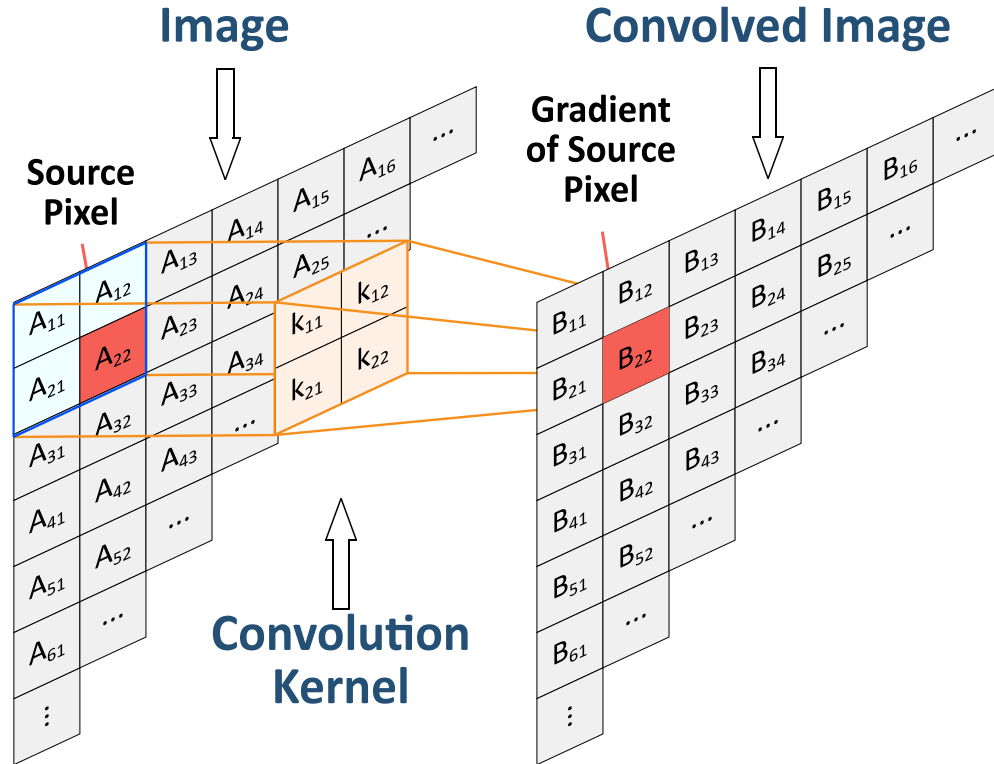
	Size [B]	Time [ms]	Energy [mJ]
FG: 1 slot	858k	16.42	15.18
FG: 2 slots	1715k	47.62	51.91
FG: 3 slots	2573k	75.95	67.1
FG: 4 slots	3430k	106.14	94.11
CG: 4 parallel	2	0.09	0.11

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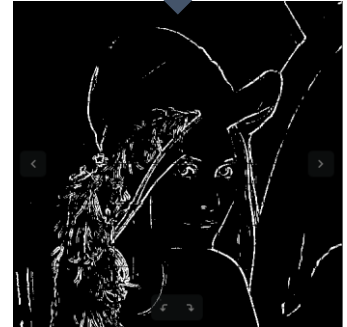
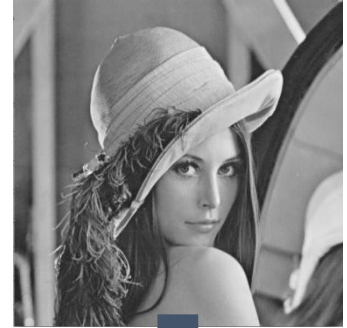
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~1000x

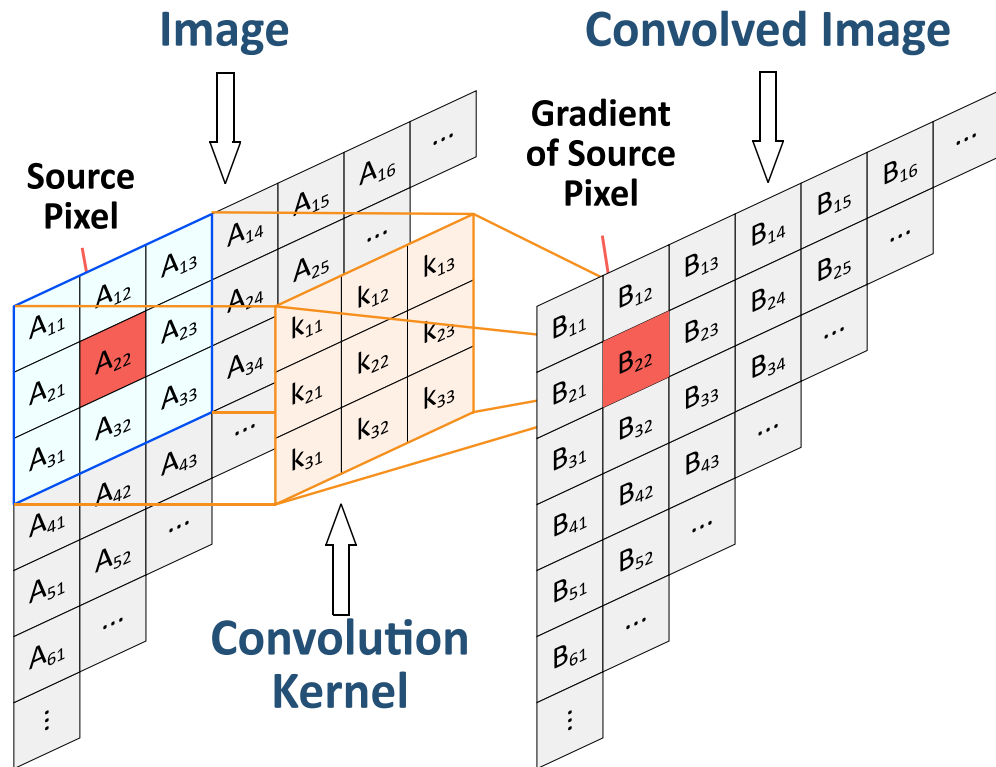
Edge Detection Application



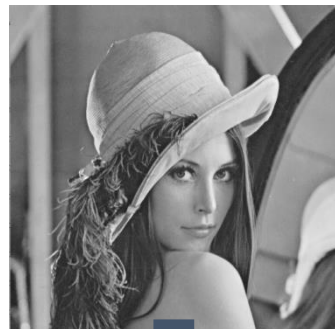
Roberts Operator



Edge Detection Application

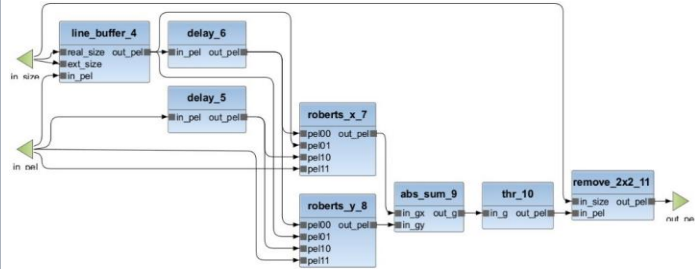


Sobel Operator

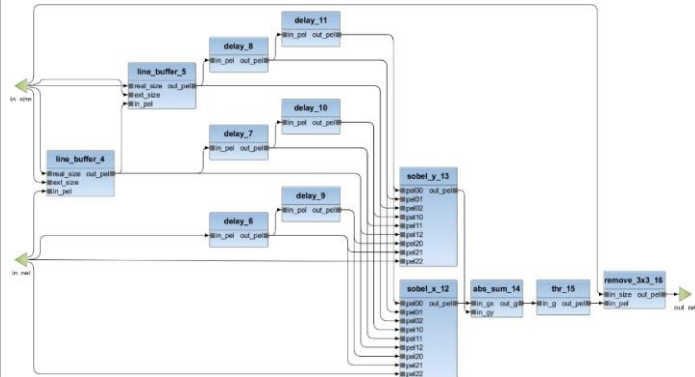


Proof of Concept: Edge Detection Application

Standalone Roberts

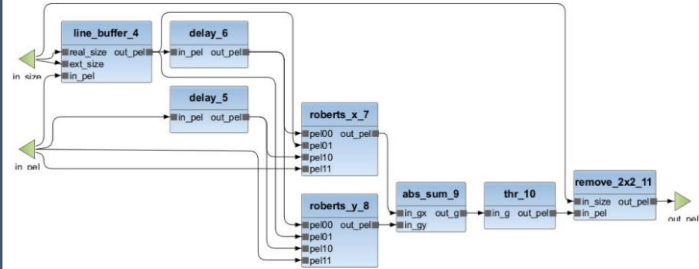


Standalone Sobel

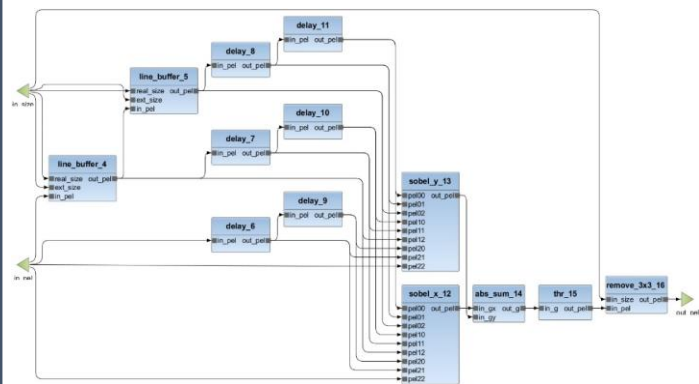


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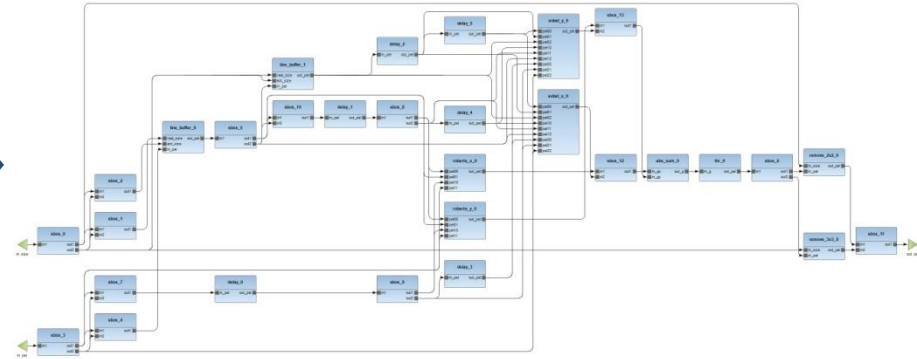
Standalone Roberts



Standalone Sobel

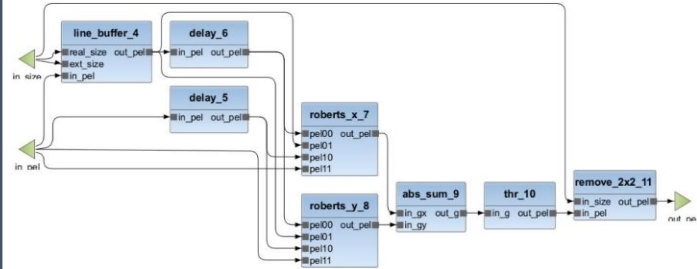


Coarse-Grain Reconfigurable (Sobel+Roberts)

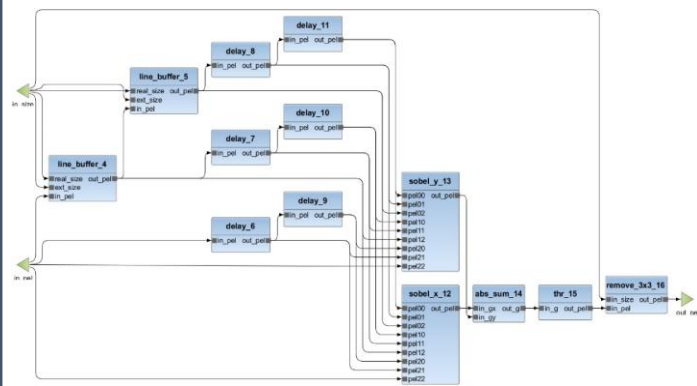


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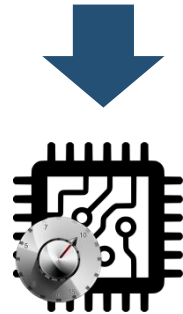
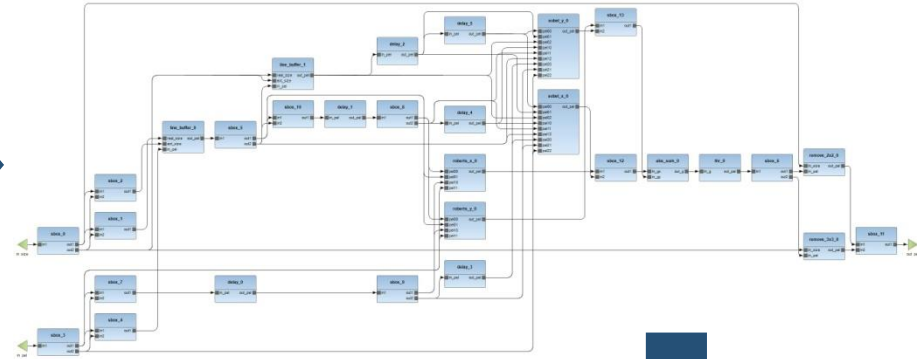
Standalone Roberts



Standalone Sobel

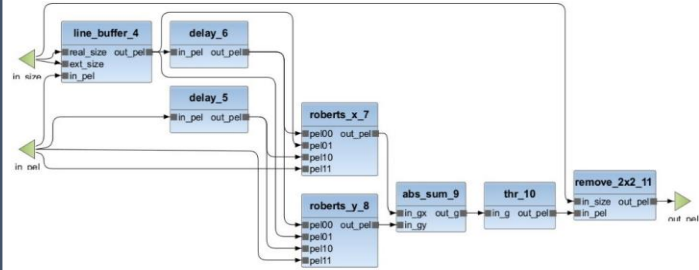


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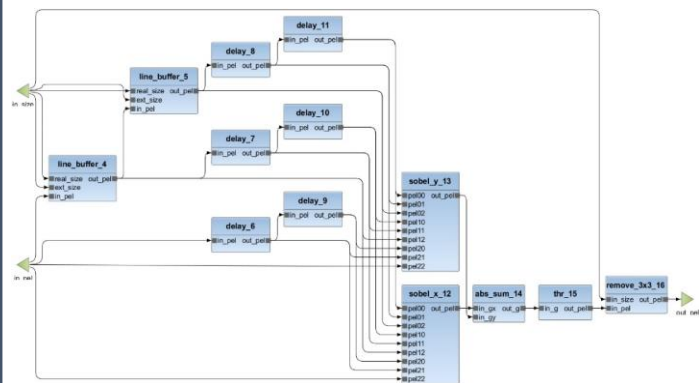


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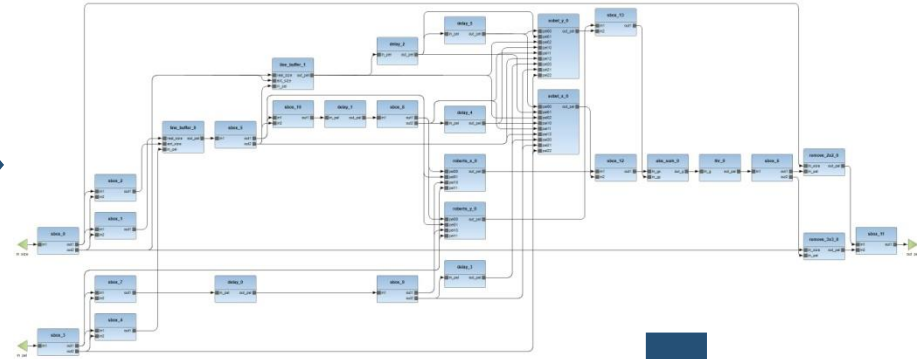
Standalone Roberts



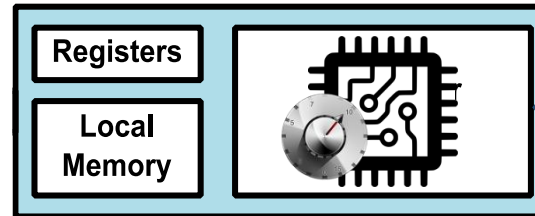
Standalone Sobel



Coarse-Grain Reconfigurable (Sobel+Roberts)



Tunable ARTICo³ slot

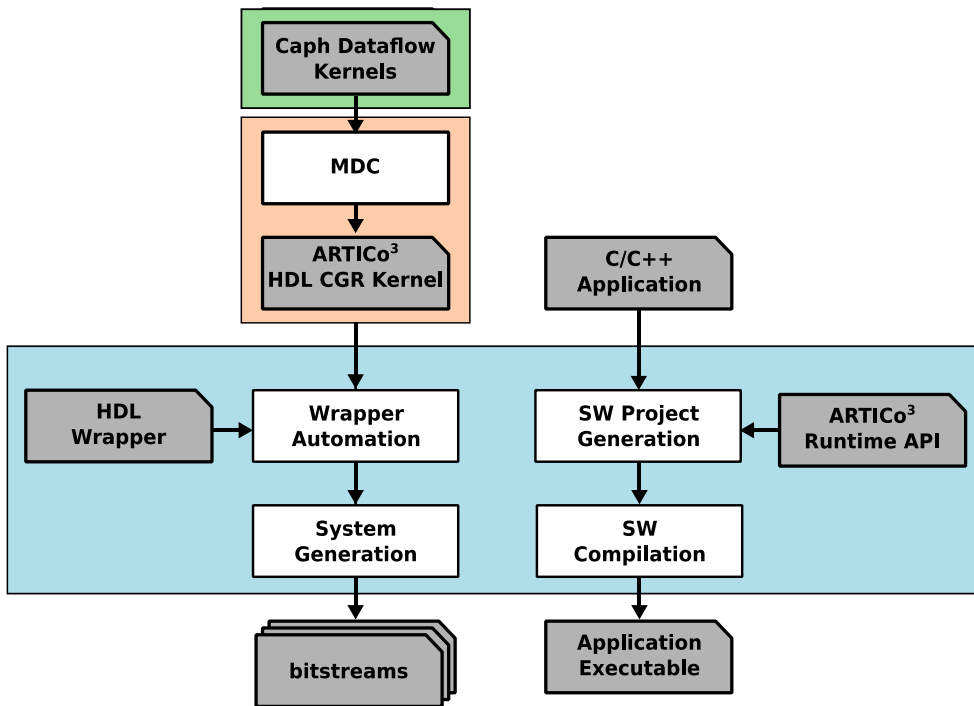


Assessed Configurations

Dataflow-to-hardware

System Implementation

Validation on FPGA

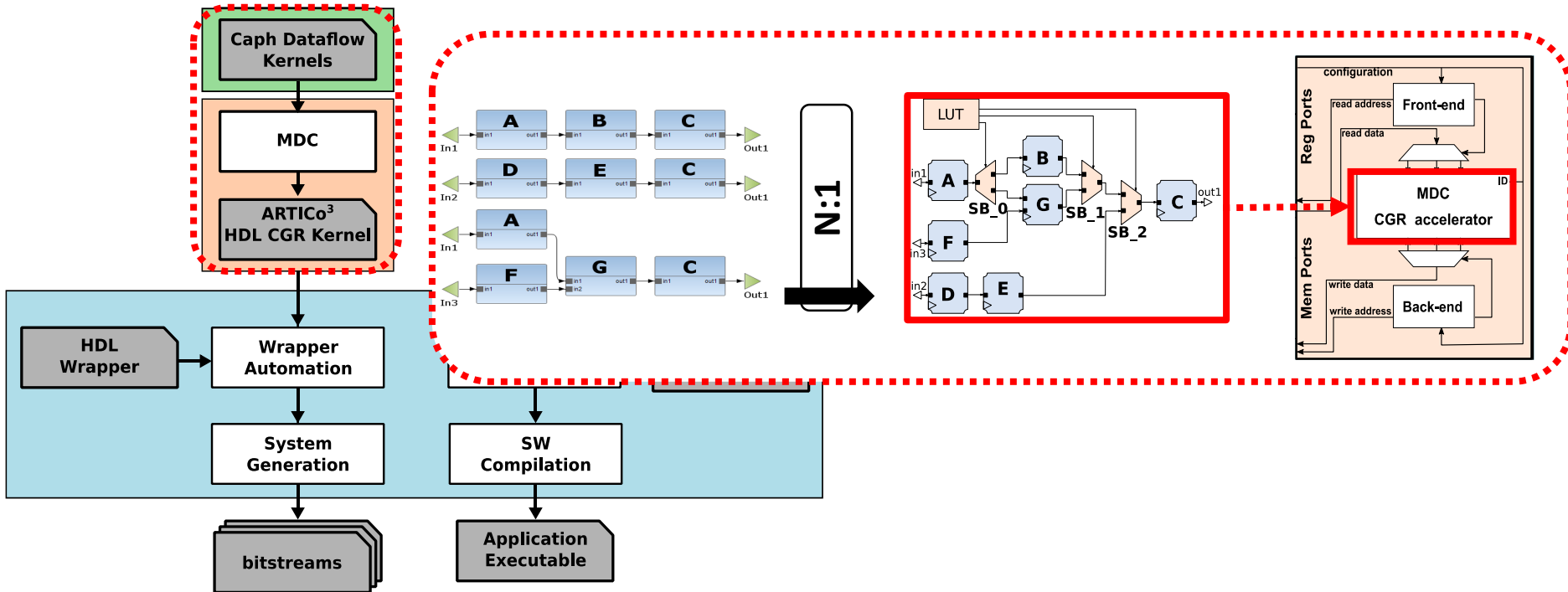


Assessed Configurations

Dataflow-to-hardware

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Validation on FPGA



Assessed Configurations

Dataflow-to-hardware

Caph Dataflow
Kernels

MDC

ARTICo³
HDL CGR Kernel

HDL
Wrapper

Wrapper
Automation

System
Generation

bitstreams

C/C++
Application

SW Project
Generation

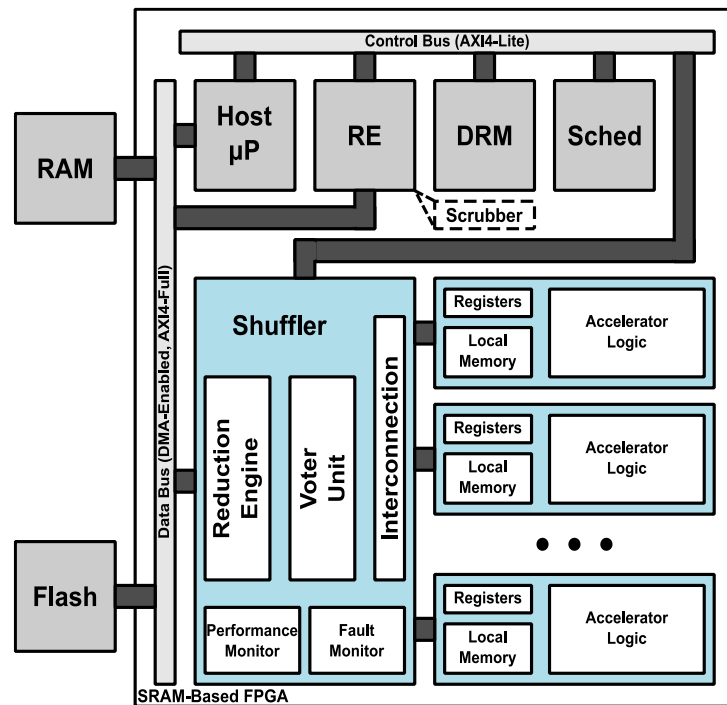
SW
Compilation

Application
Executable

ARTICo³
Runtime API

System Implementation

Validation on FPGA

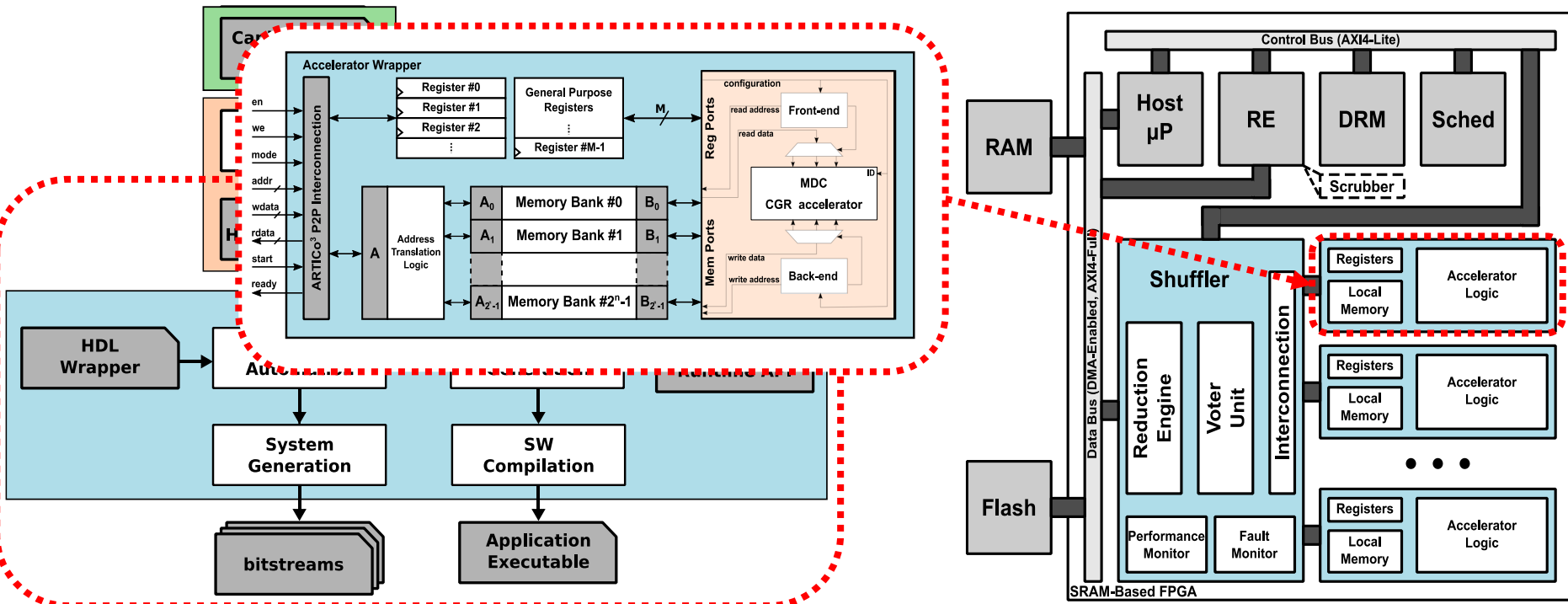


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*Dataflow-to-
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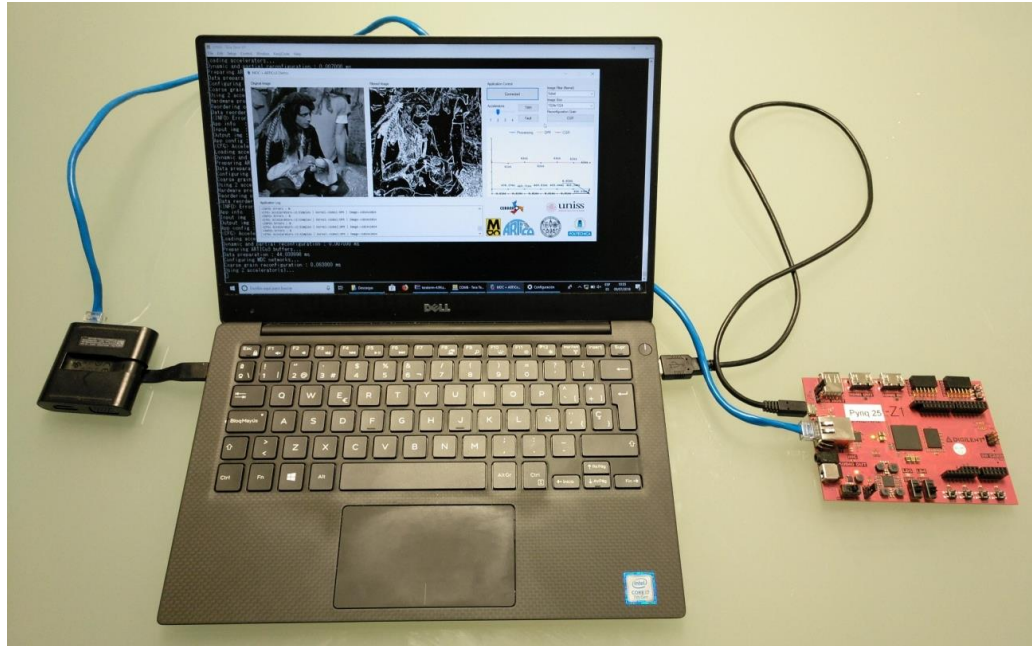


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Tutorial time...



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