Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems

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The H2020 CERBERO European Project aims at developing a continuous design environment for CPS, including modelling, deployment and verification (http://www.cerbero-h2020.eu/). The efficient support for runtime reconfiguration, taking into account an uncertain environment with changing requirements, is among the CERBERO expected outcomes. In CERBERO, two tools offer support for hardware reconfiguration. The ARTICo^3 framework provides adaptive and scalable hardware acceleration by using Dynamic Partial Reconfiguration (DPR) [1]. The MDC design suite, on the other hand, delivers Coarse-Grained Reconfigurable (CGR) systems based on the dataflow model of computation, and has been already proved to be a viable solution to enable adaptivity in CPS [2]. The integration of ARTICo^3 and MDC combines together the benefits from both DPR and CGR, leading to the implementation of flexible systems that can adapt to the changing requirements of most CPS scenarios. Figure 1 shows the integrated design flow: it starts from high-level descriptions of the functionalities to be implemented; the integrated toolchain derives the corresponding CGR HDL computational kernel and wraps it with the logic necessary to serve as an ARTICo^3 DPR reconfigurable partition. Finally, the bitstreams of the system (static part) and of the hardware accelerators (reconfigurable partitions) are generated. On the software side, the toolchain has the capability, inherited from ARTICo^3, of generating the application executable that manages operation execution and computation offloading to the hardware accelerators. Bottom part of Figure 1 depicts an example of the implemented multi-grain reconfigurable architecture providing scalable parallelism through DPR and fast functional reconfiguration with CGR.

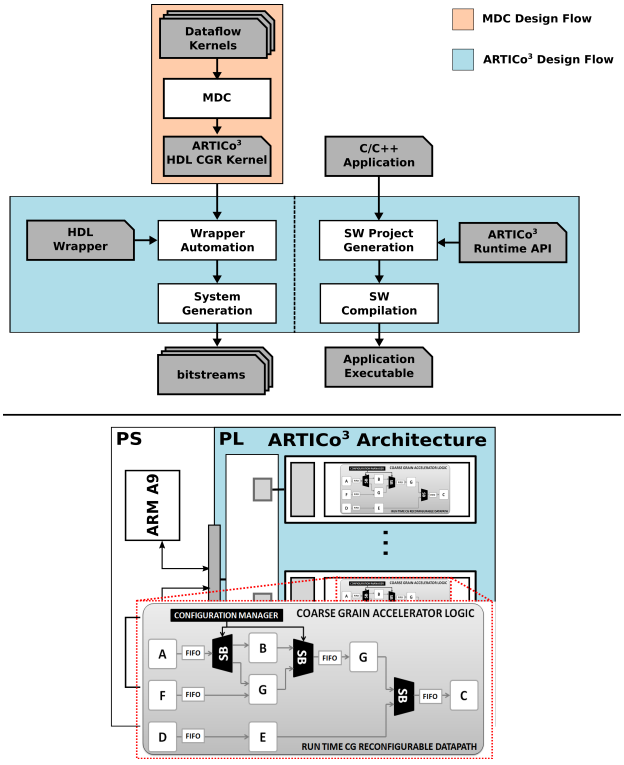

Fig. 1. Integrated Toolchain for Multi-Grain Reconfigurable Systems Design

Tutorial Description

This tutorial shows the multi-grain reconfiguration capabilities of the combined MDC-ARTICo^3 flow in an image-processing application scenario, and it is divided in three parts:

1) Composition of the dataflow-based ARTICo^3 compliant CGR accelerators, adopting MDC Tool.
2) Composition of DPR-enabled computing systems, using the CGR-based accelerators and the ARTICo^3 framework.
3) Running on Board. In order to switch from one kernel to another, the user can decide to use the DPR approach of ARTICo^3 to completely change the logic instantiated in each slot, or to use the CGR approach of the MDC-generated accelerators to multiplex the internal datapath of the accelerators.

As a result, it is possible to see, in real time, the runtime overheads of each type of reconfiguration mechanism. Additional adaptivity evaluation can be performed by changing the working point of the application, which is based on several parameters: input image size, number of hardware accelerators used to exploit data-level parallelism.

References

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[2] F. Palumbo *et al.*, "Power-awarness in coarse-grained reconfigurable multi-functional architectures: a dataflow based strategy," *Journal of Signal Processing Systems*, pp. 1–26, 2016.