Centro de Electrónica Industrial - UPM
30 May 2018

Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems

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Università degli Studi di Cagliari

Horizon 2020
European Union funding
for Research & Innovation

Who and Where

Who and Where

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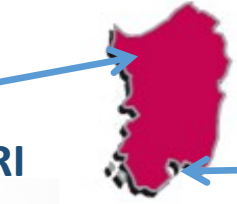

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Who and Where

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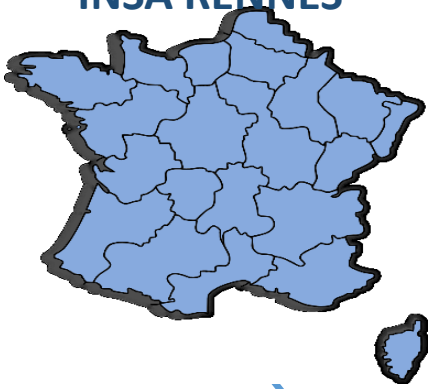

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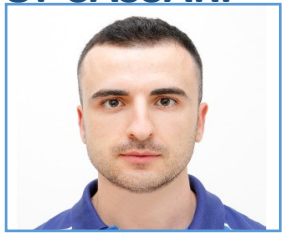

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…and What

Reconfigurable systems design and development of code generation tools for low power reconfigurable hardware architectures.

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Outline

- Concepts & Definition
  - Self-Adaptation in Cyber-Physical Systems
  - Types of Adaptation
  - The Adaptation Loop
- Adaptive CPS: The CERBERO approach
  - Self-Adaptation in CERBERO H2020
  - Adaptation Fabrics in CERBERO H2020
- HW Adaptation in CERBERO
  - ARTICo3
  - MDC-compliant CG adaptation
- Mixed-Grain Adaptivity
  - ARTICo3 + MDC integration
- Next-steps
  - Monitoring
  - Adaptivity Support

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Self-Adaptation in Cyber-Physical Systems

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ENVIRONMENTAL AWARENESS: Influence of the environment on the system, i.e. daylight vs. nocturnal, radiation level changes, etc.

Sensors are needed to interact with the environment and capture conditions variations.

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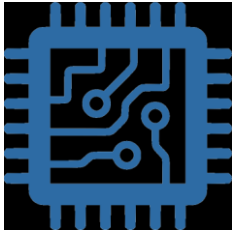
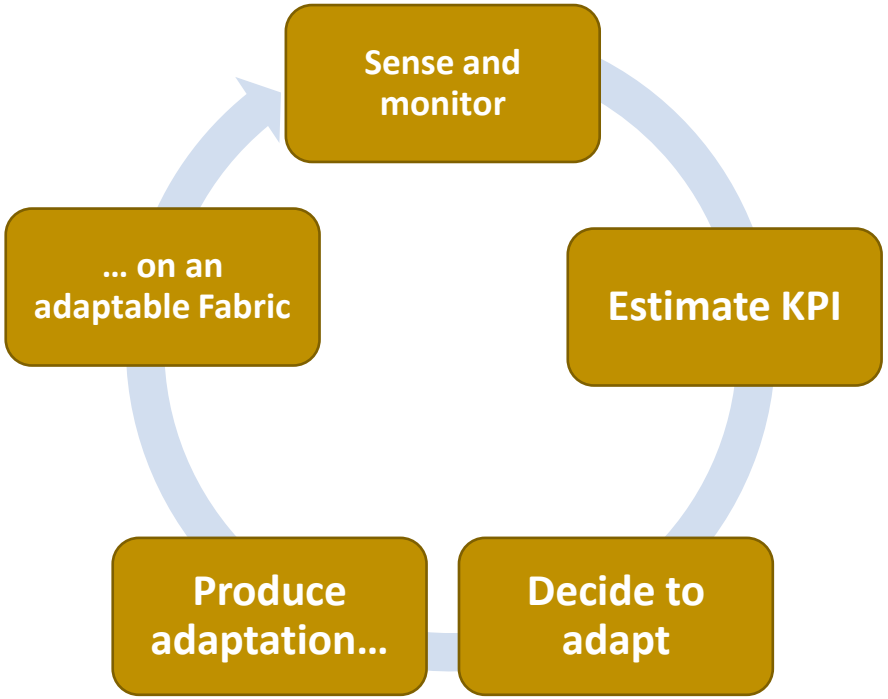


SELF-AWARENESS: The internal status of the system varies while operating and may lead to reconfiguration needs, i.e. chip temperature variation, low battery.
Status monitors are needed to capture the status of the system.

Adaptation Loop



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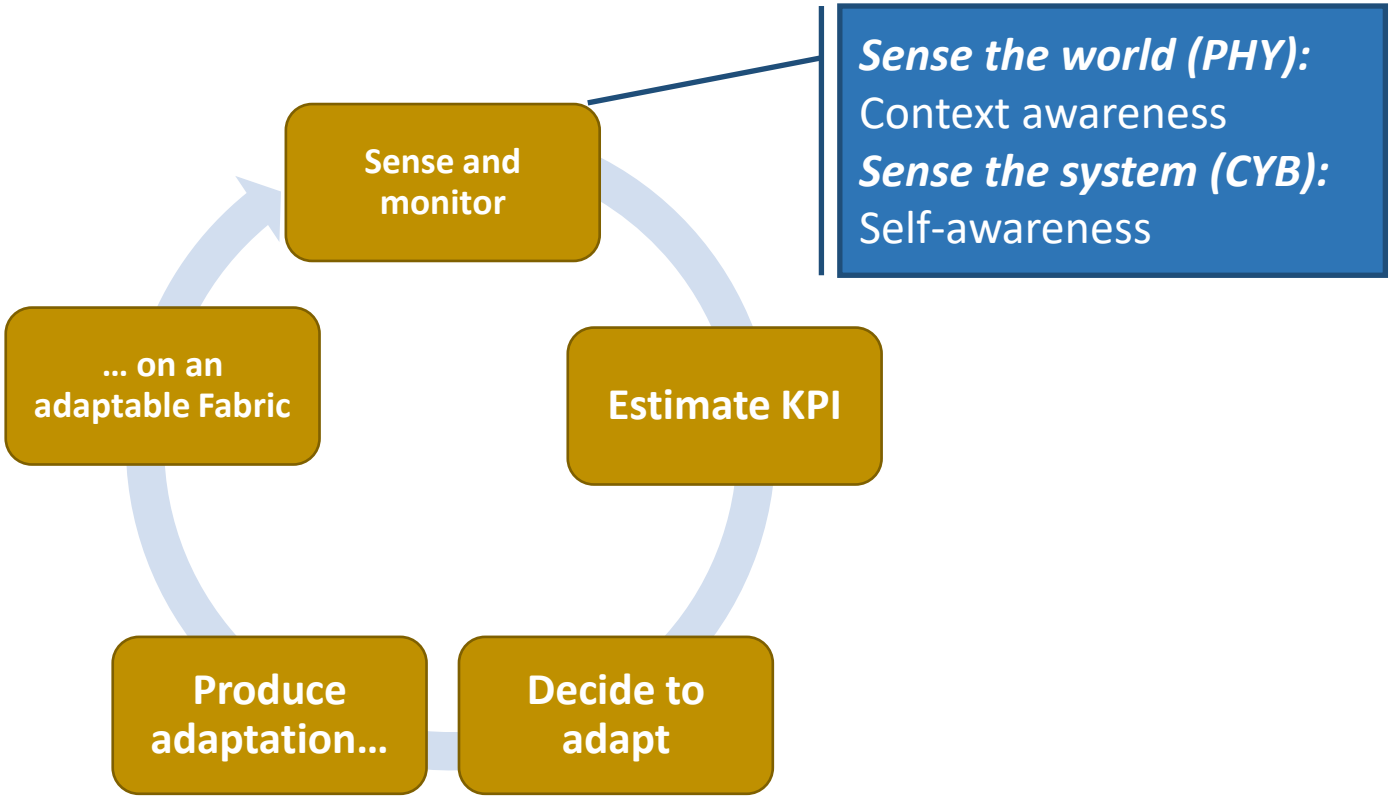

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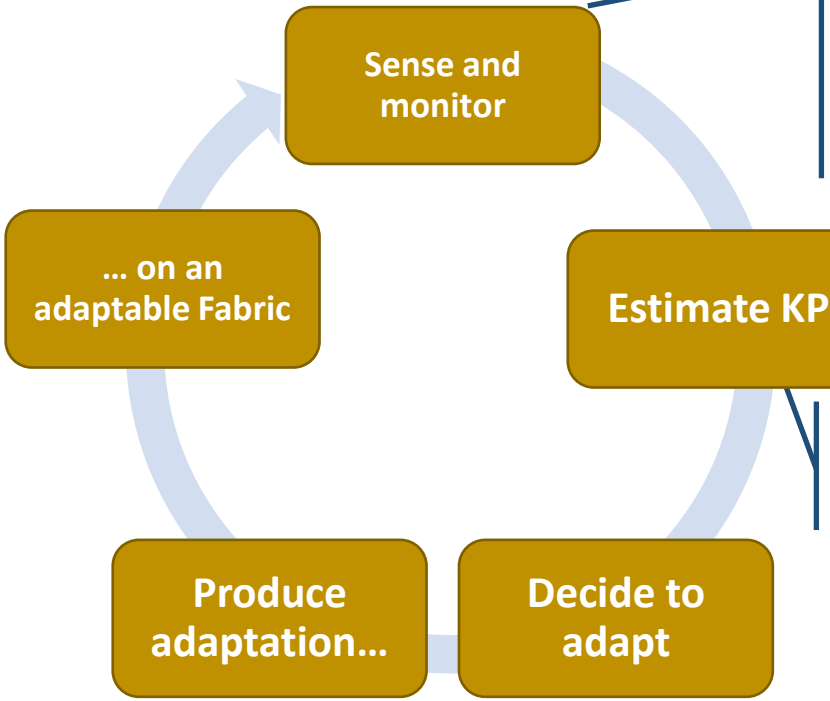
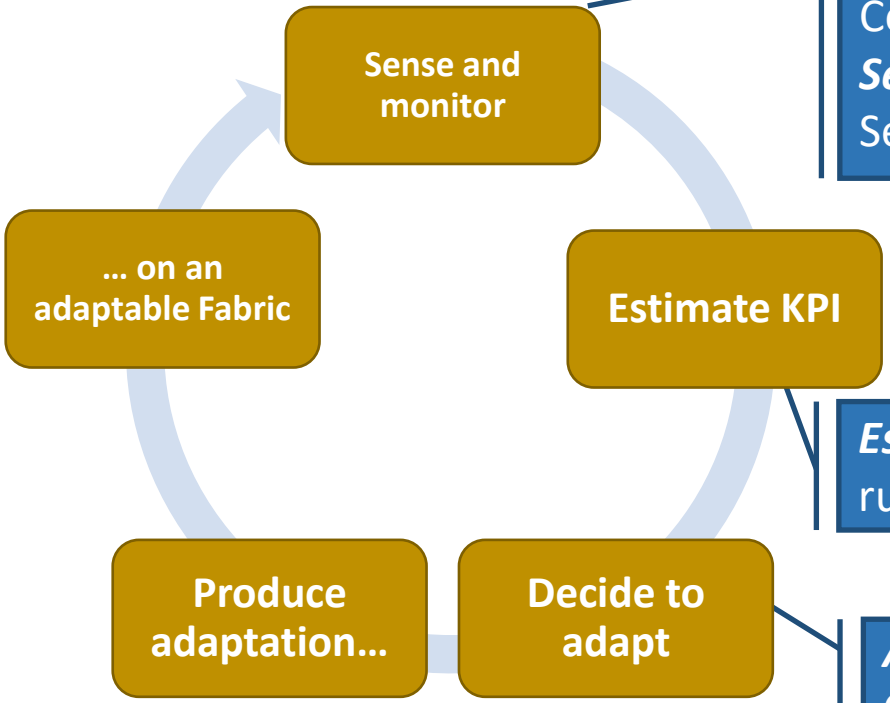


Sense the world (PHY):
Context awareness
Sense the system (CYB):
Self-awareness

Estimate Performance:
runtime models

Adaptation Loop



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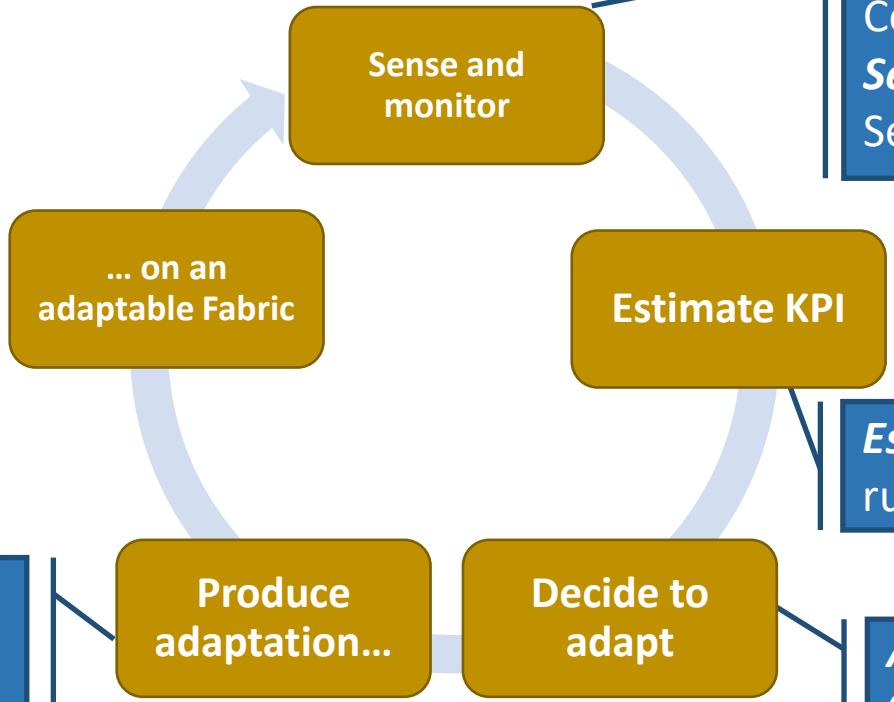

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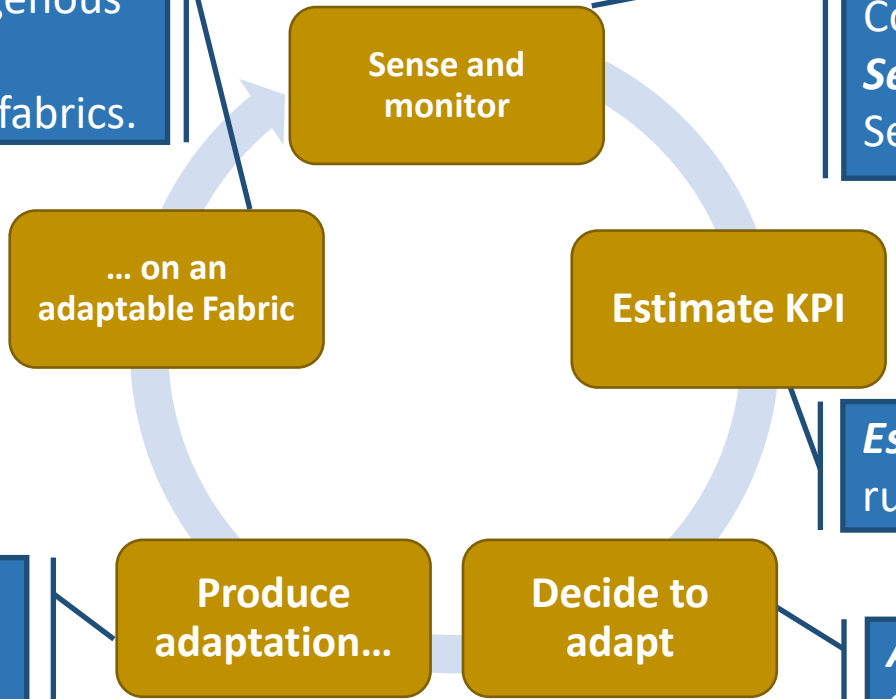

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Command Adaptation:
Put in place the actions for the required adaptation

Adapt:
Reconfigure the heterogenous (HW-SW) computing infrastructure. Multiple fabrics.

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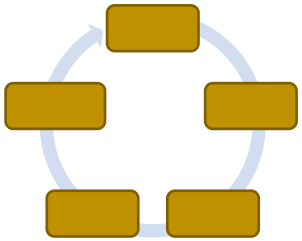
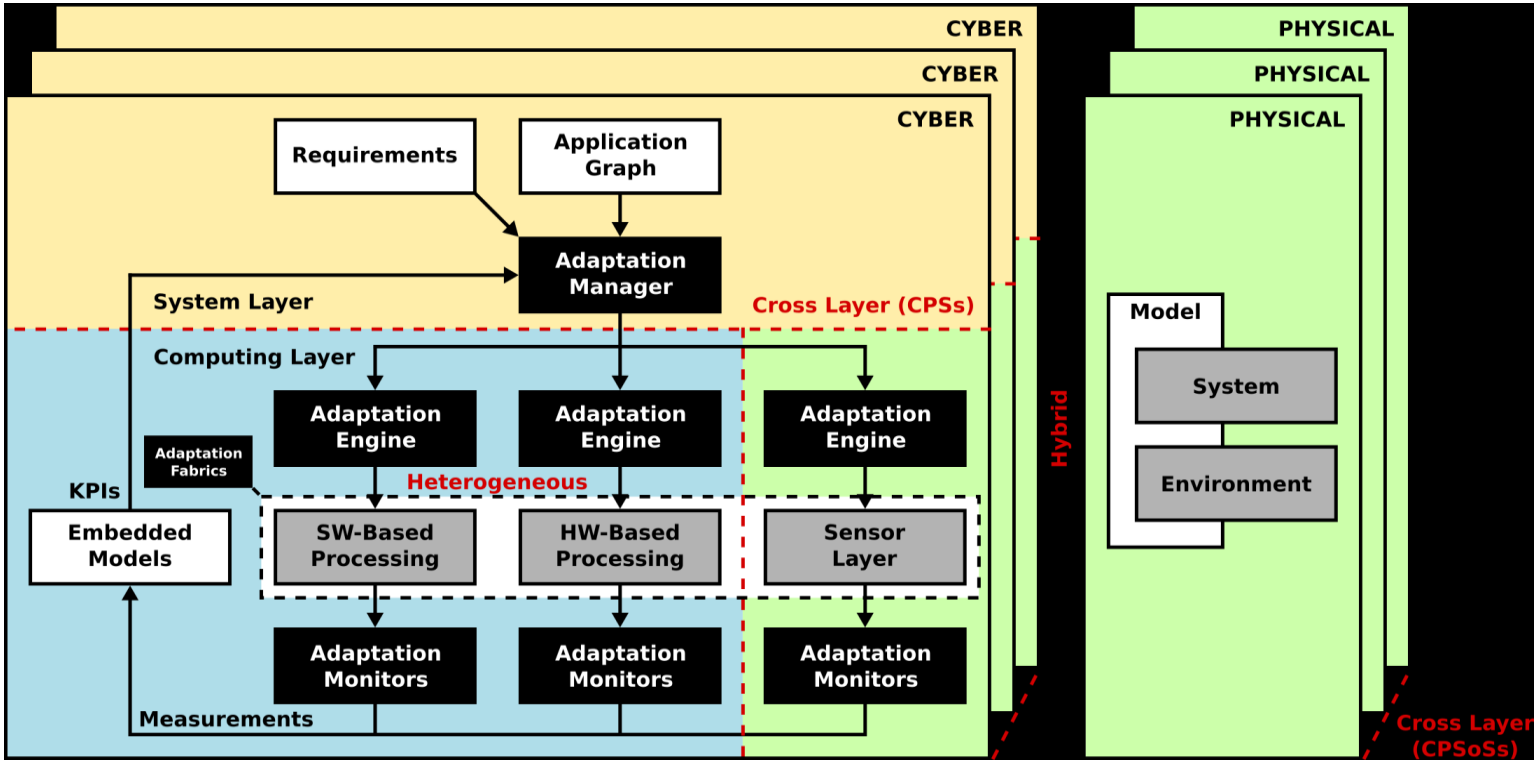
Self-Adaptation in CERBERO H2020





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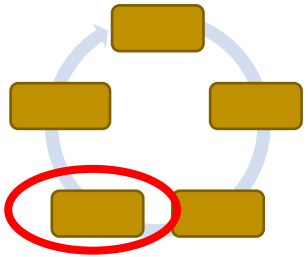

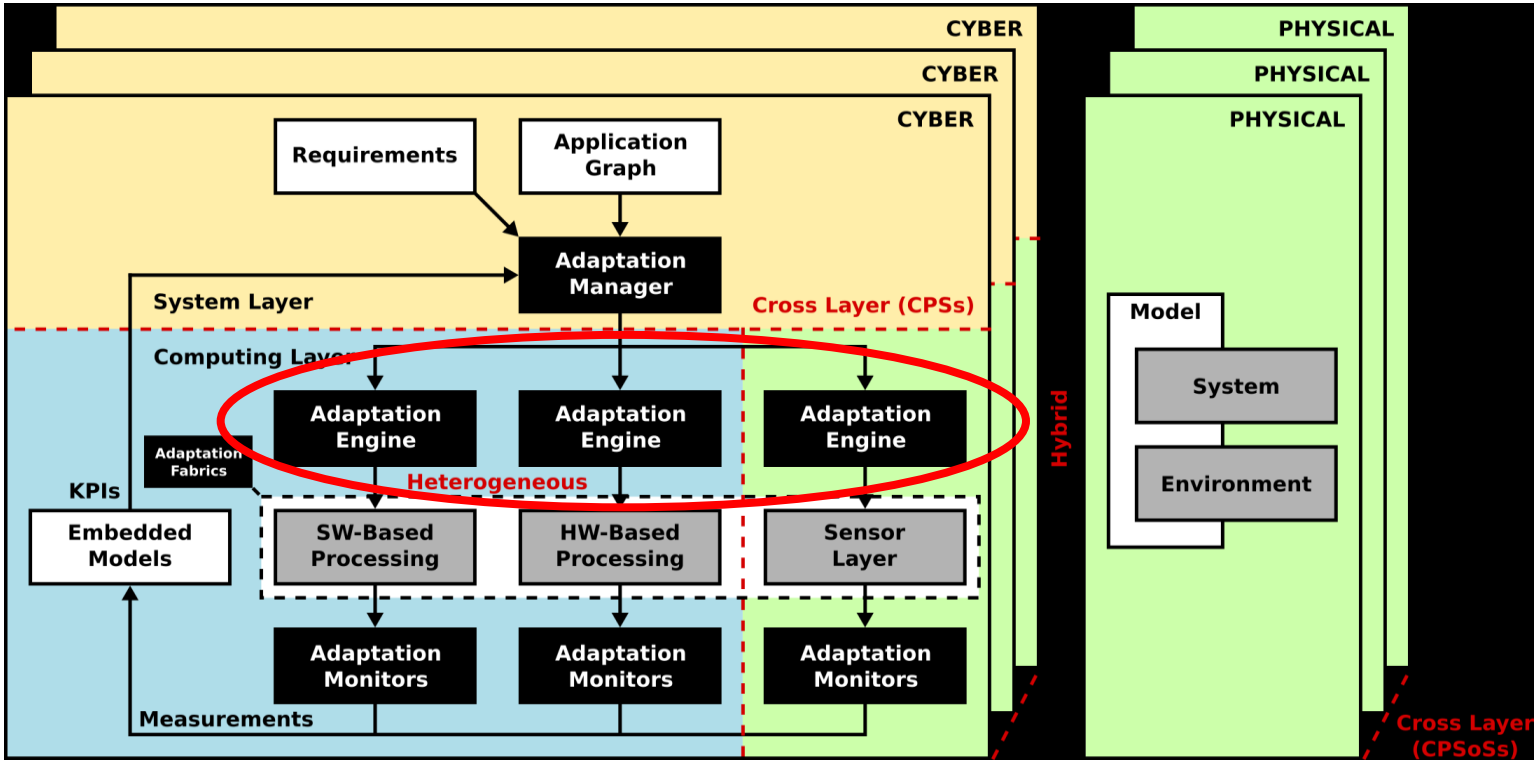

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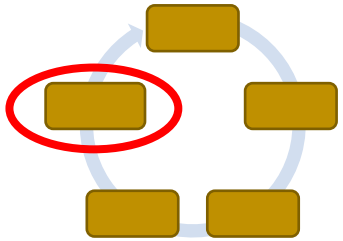

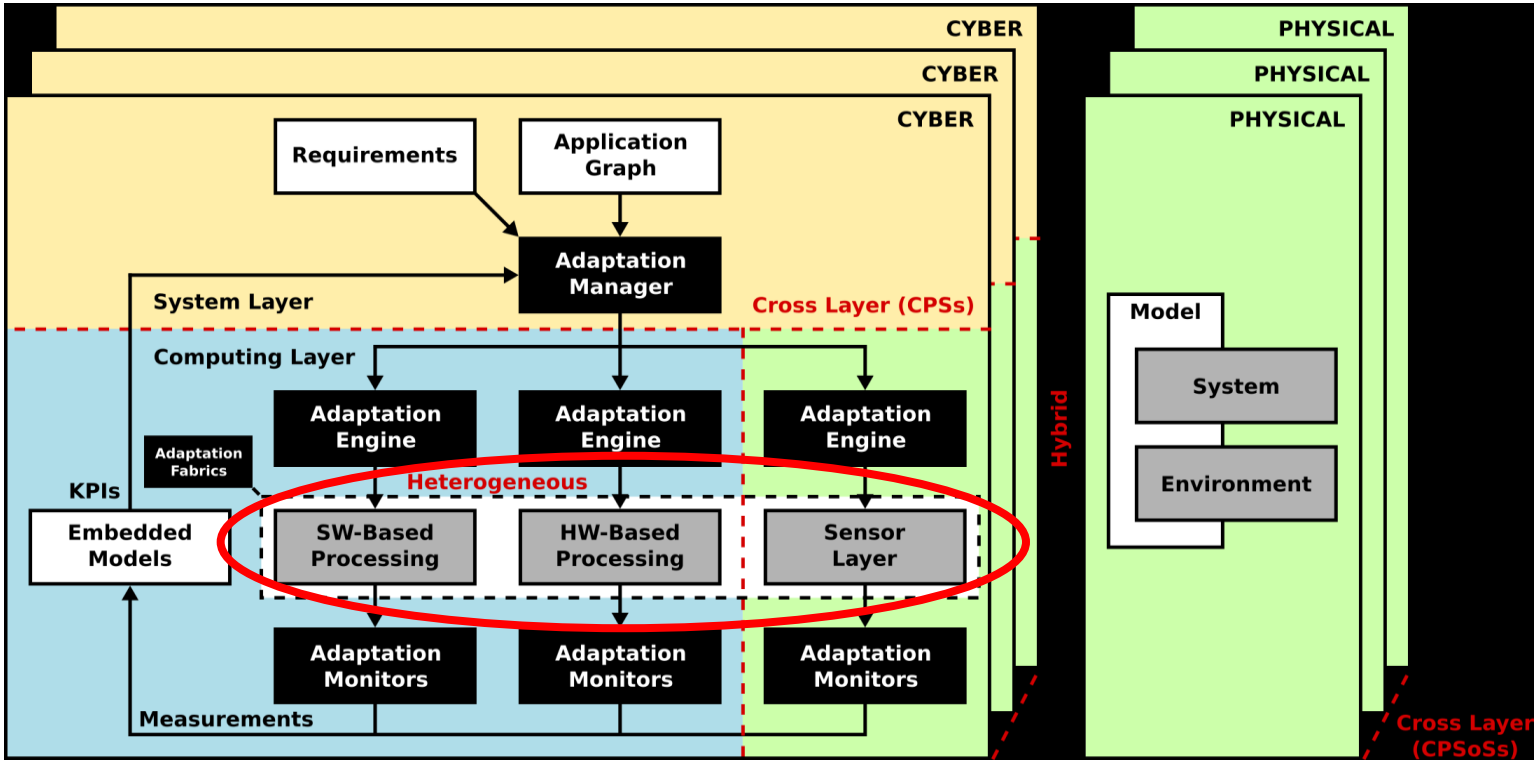

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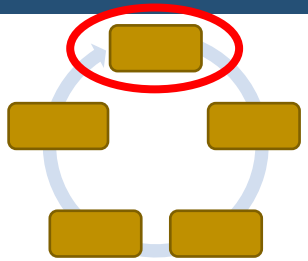

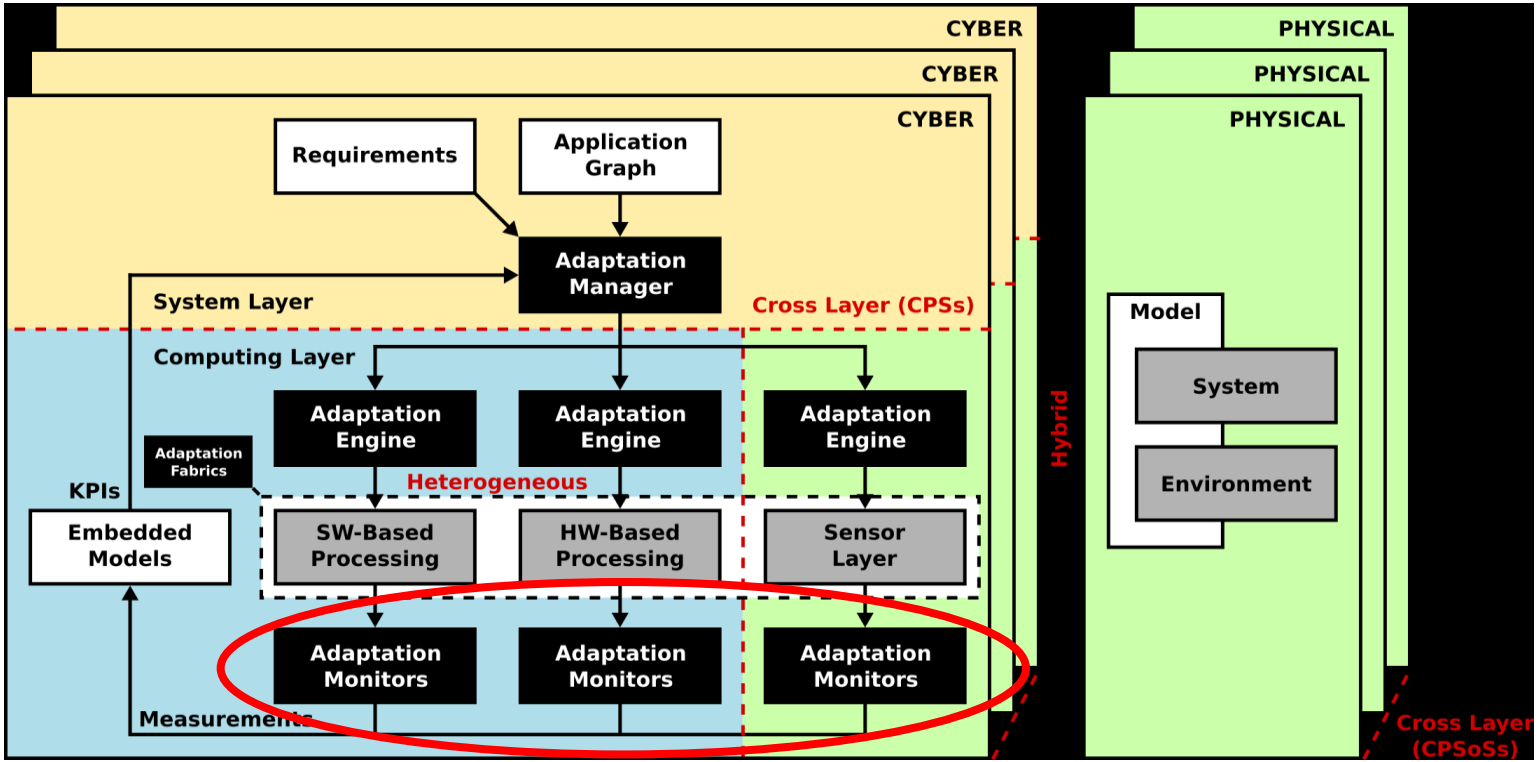

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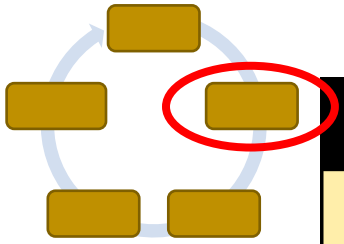

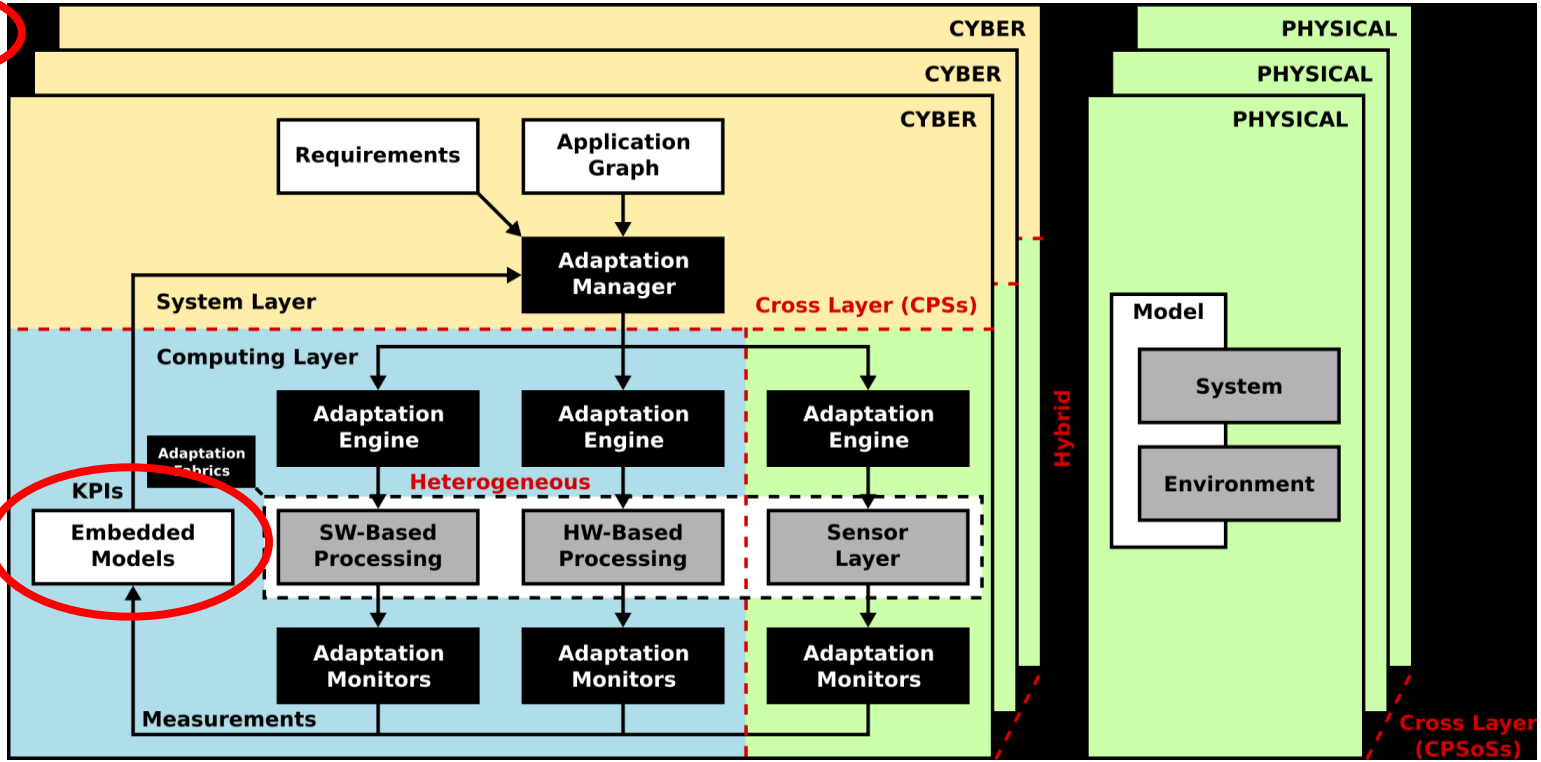

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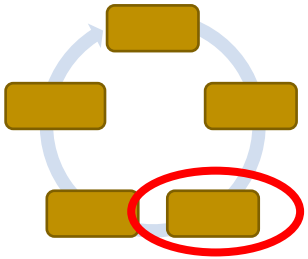

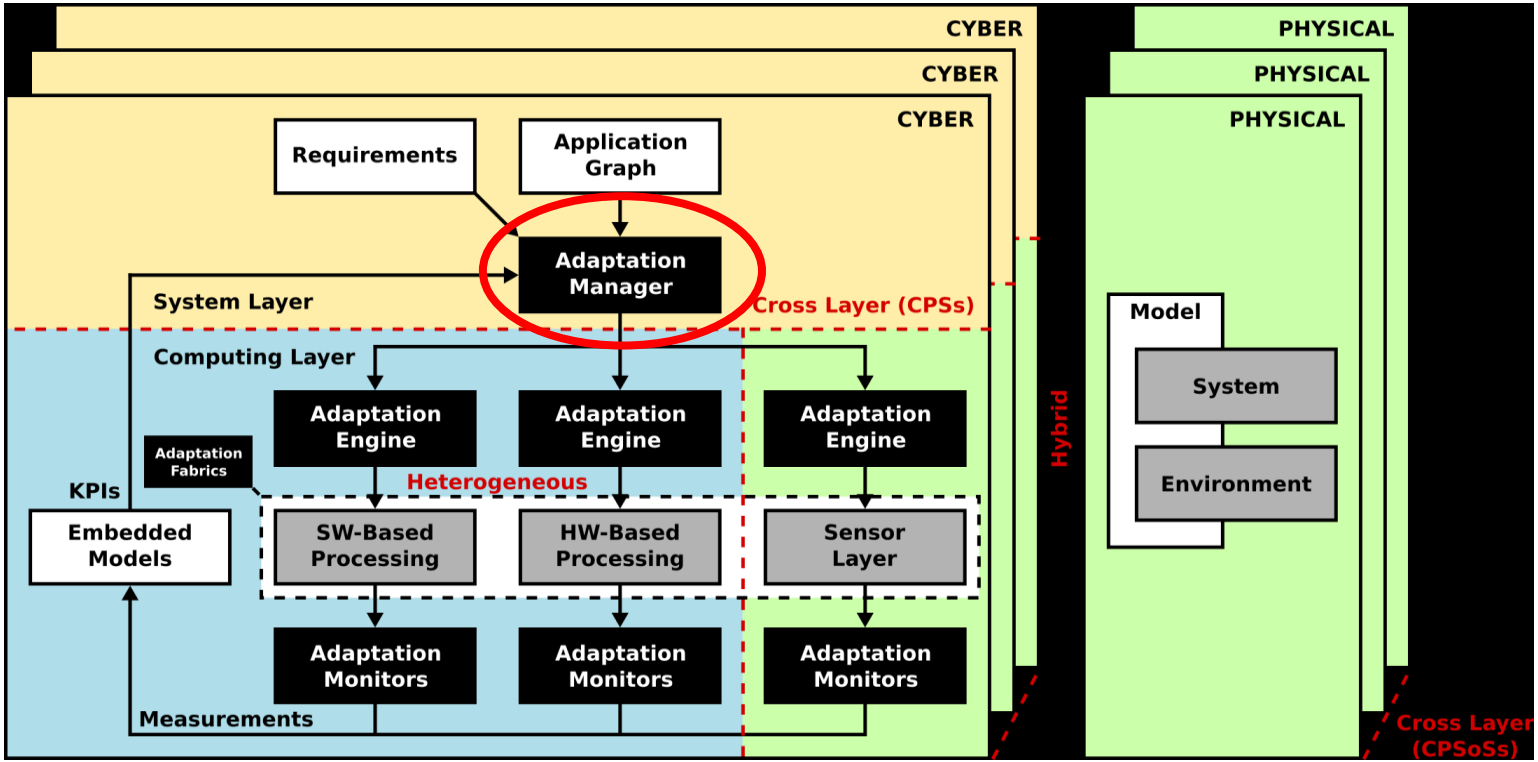

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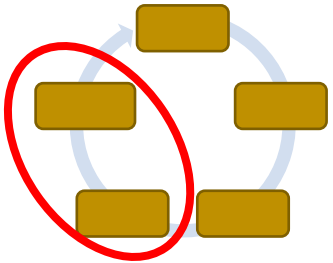

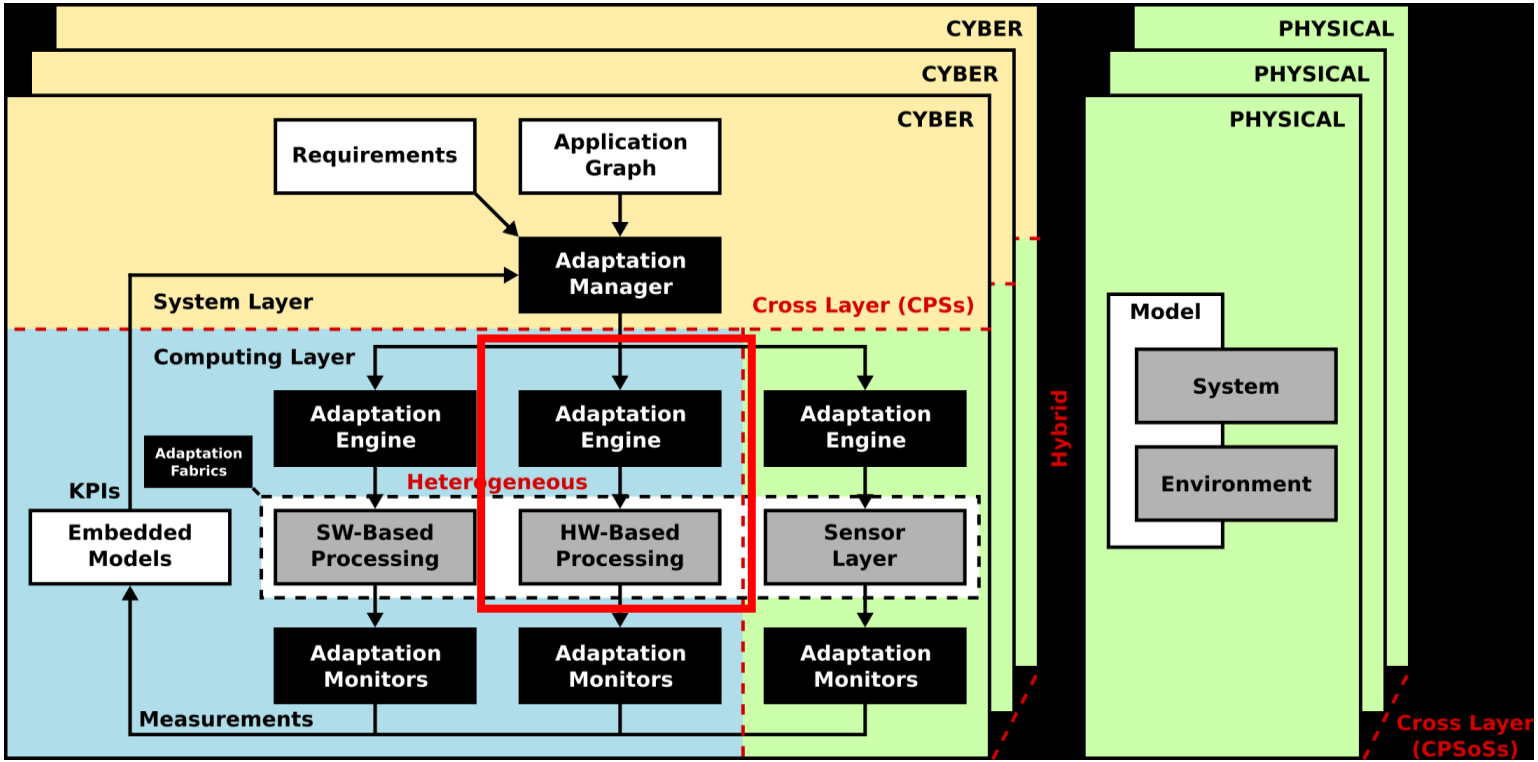

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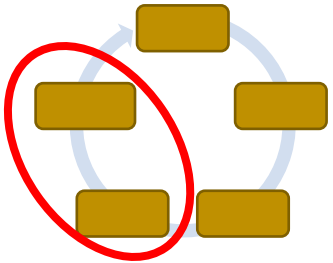
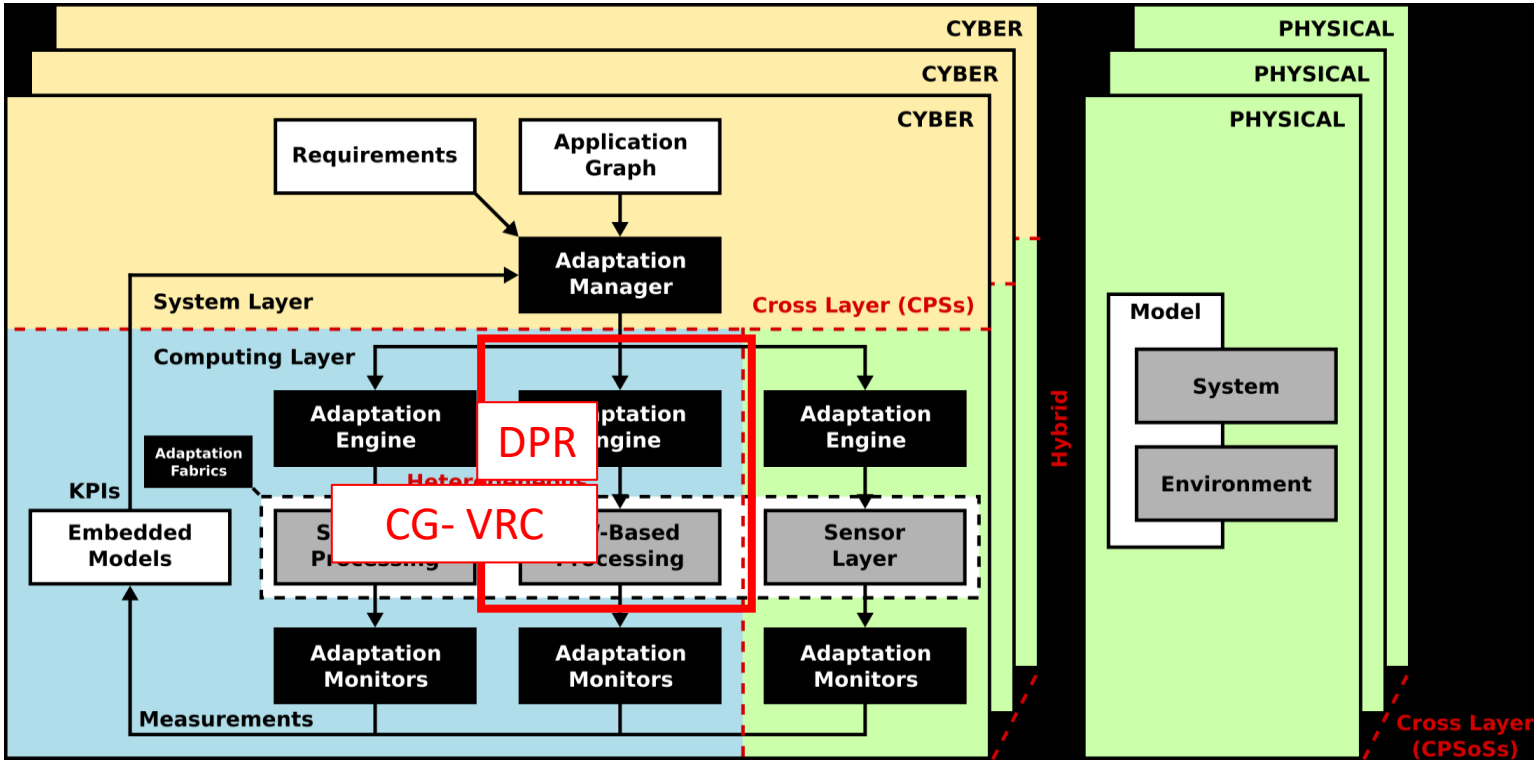
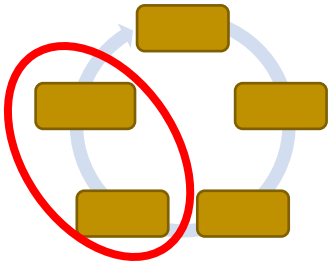
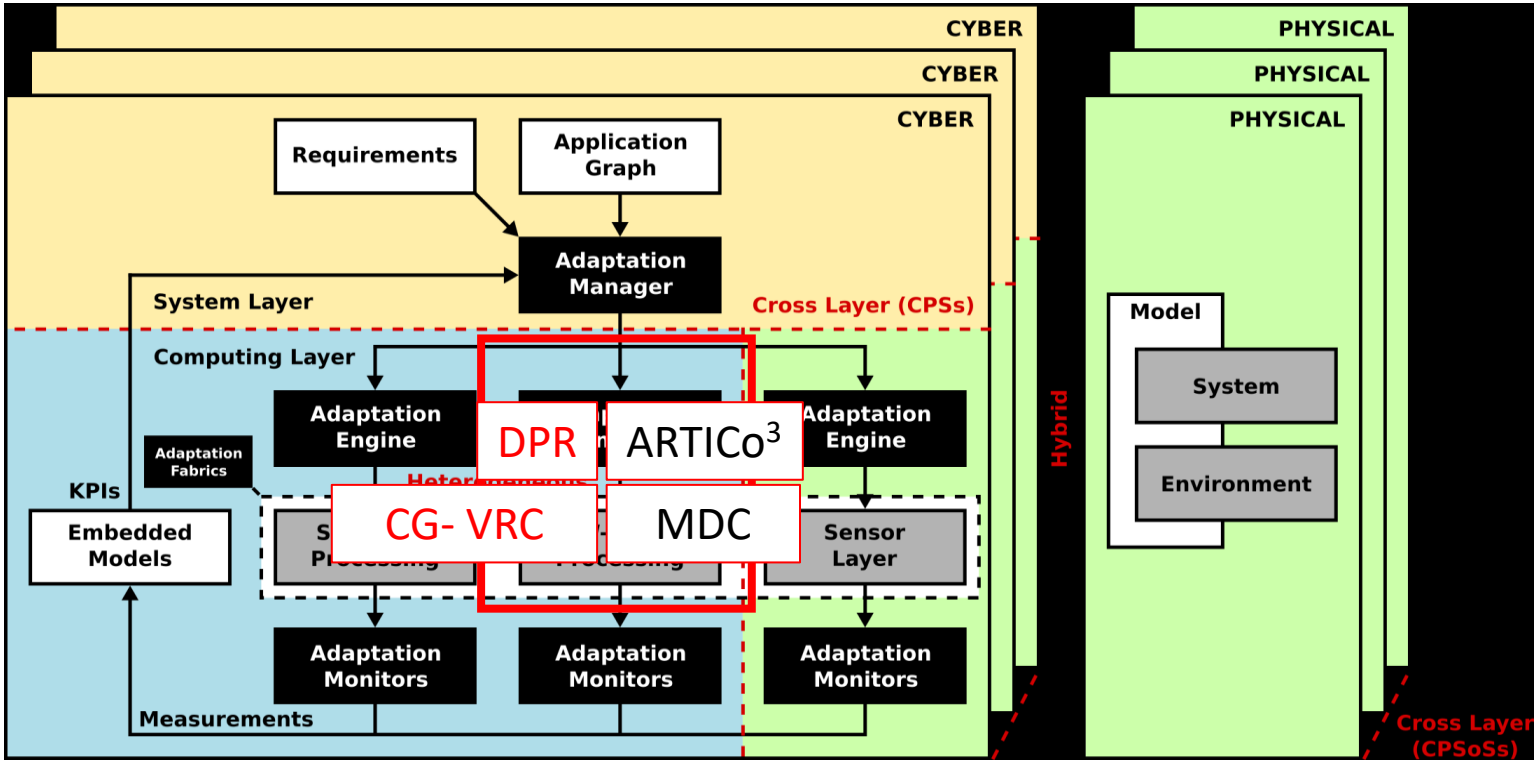




Adaptation fabrics in CERBERO H2020





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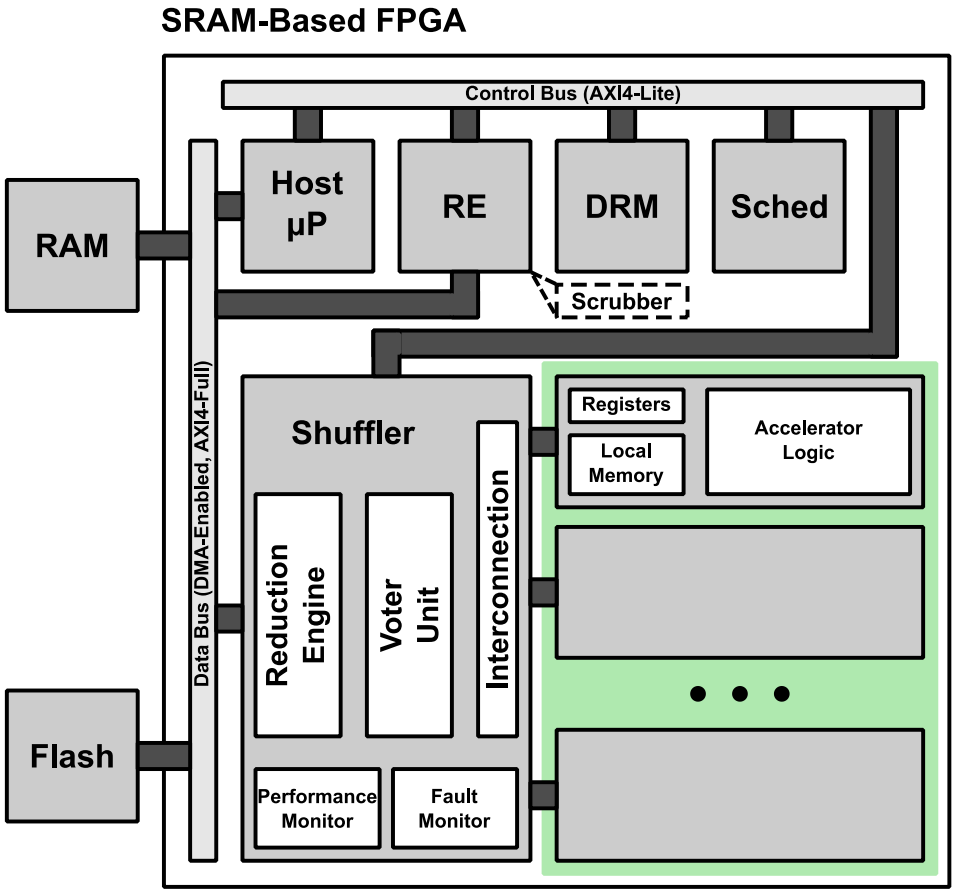
ARTICo³ Architecture



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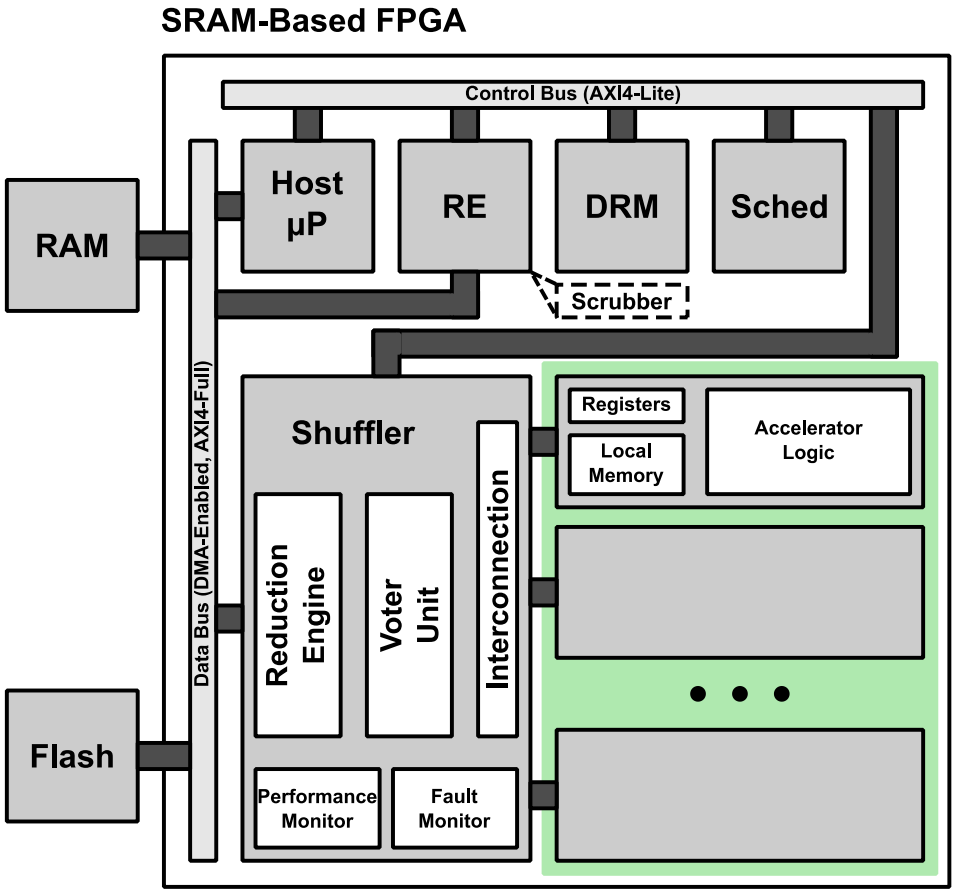

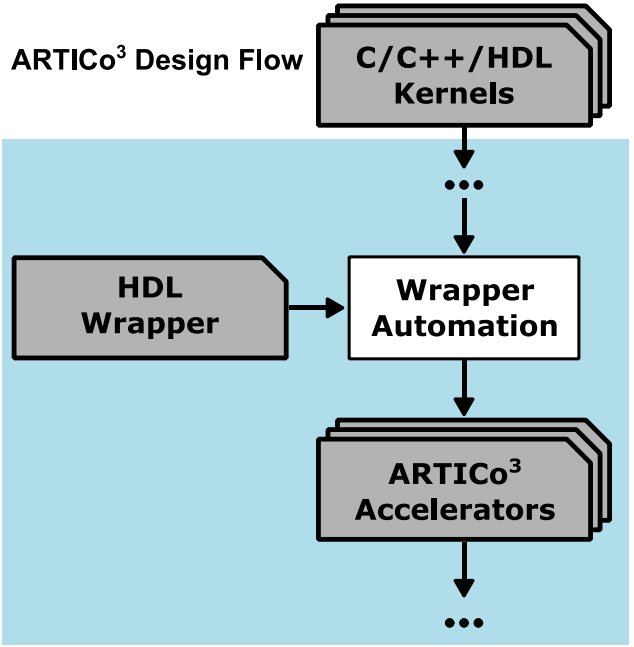

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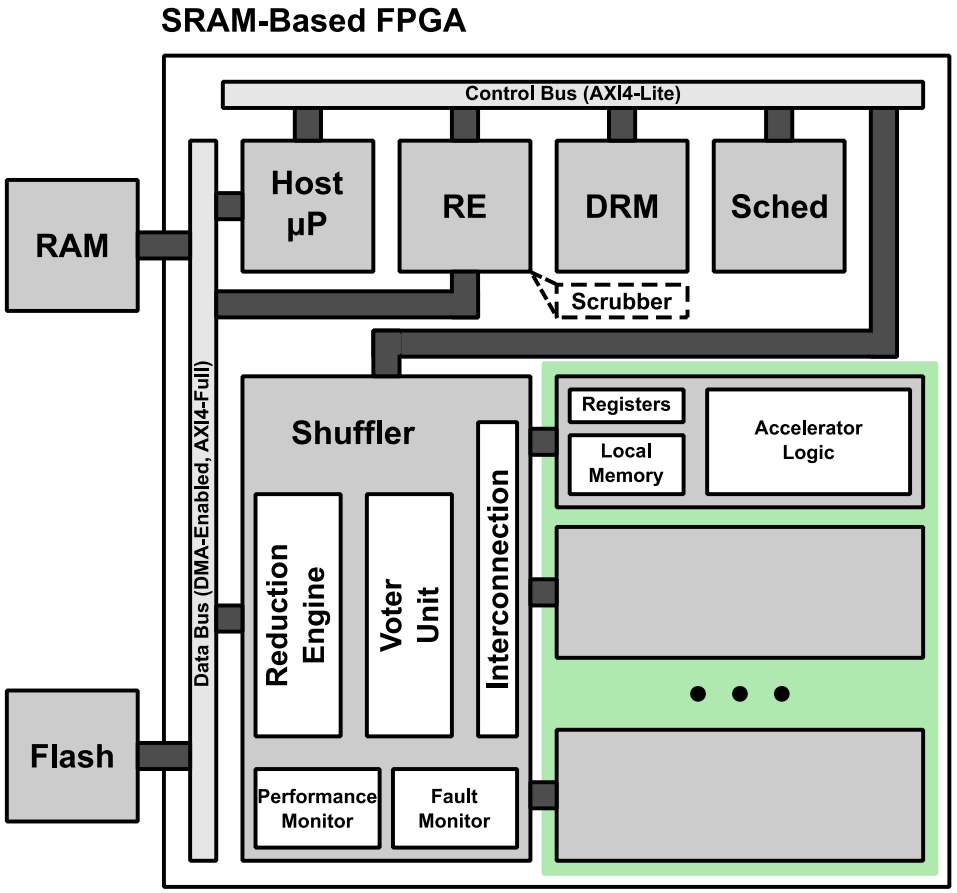

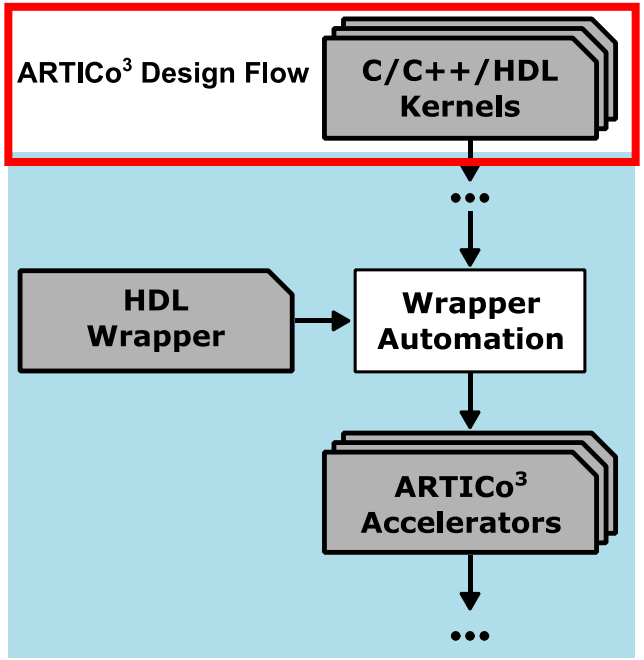

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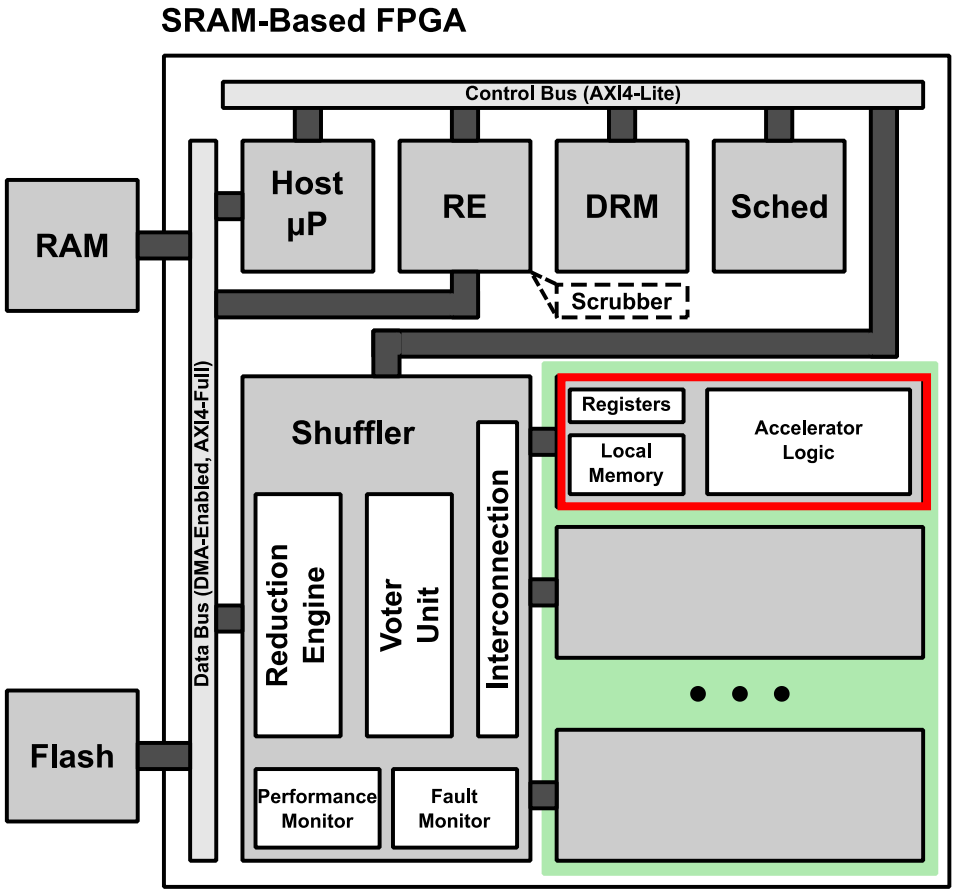

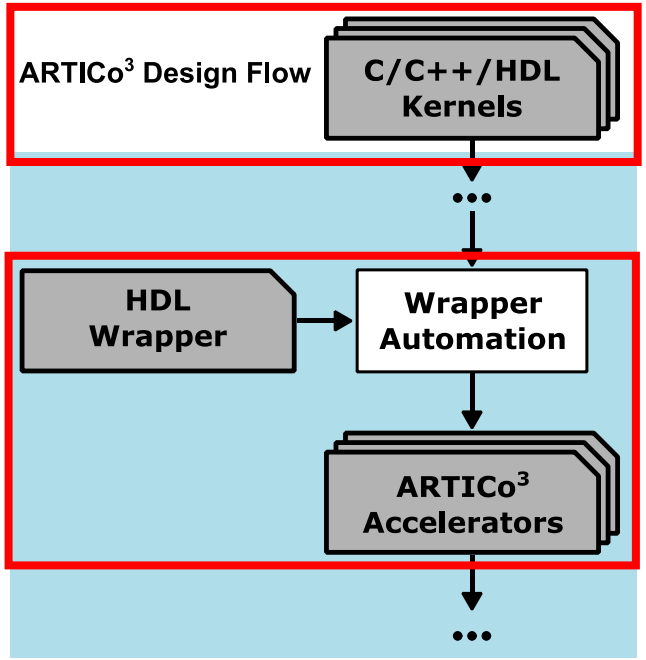

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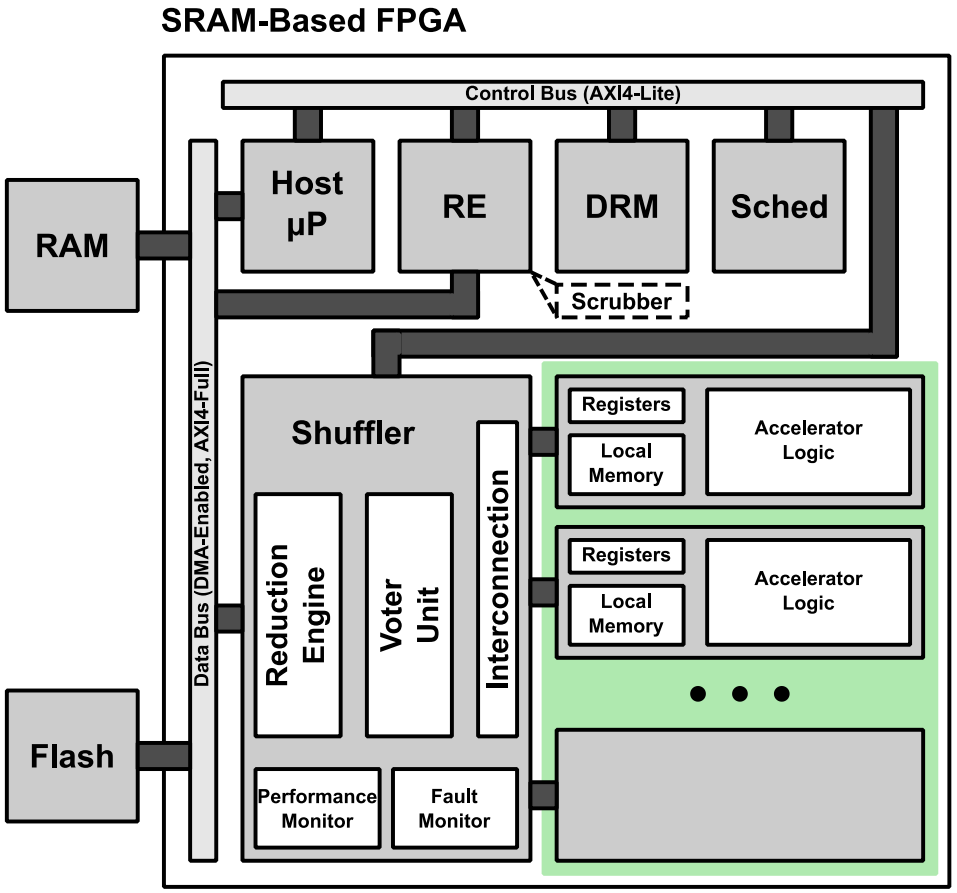

- Multiple accelerators providing performance scalability and adaptive fault tolerance
- Coalesced transactions for fast data exchange via AXI4-full
- Runtime support by ARTICo³ API
- It follows a data-parallel MoC, similar to GPUs

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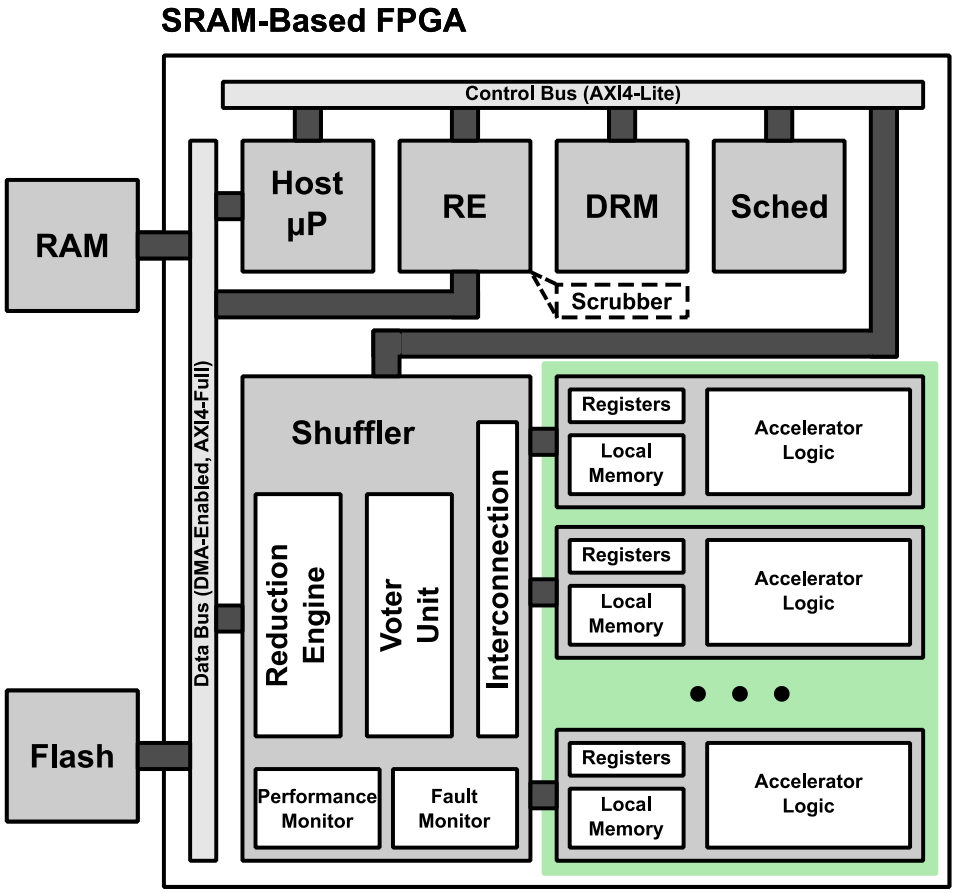

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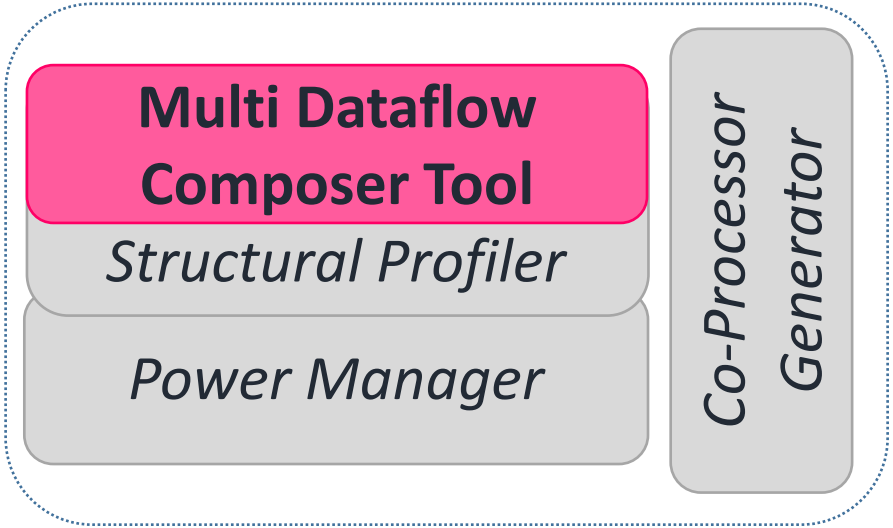
MDC tool: Dataflow to HW Mapping



MDC design suite

http://sites.unica.it/rpct/

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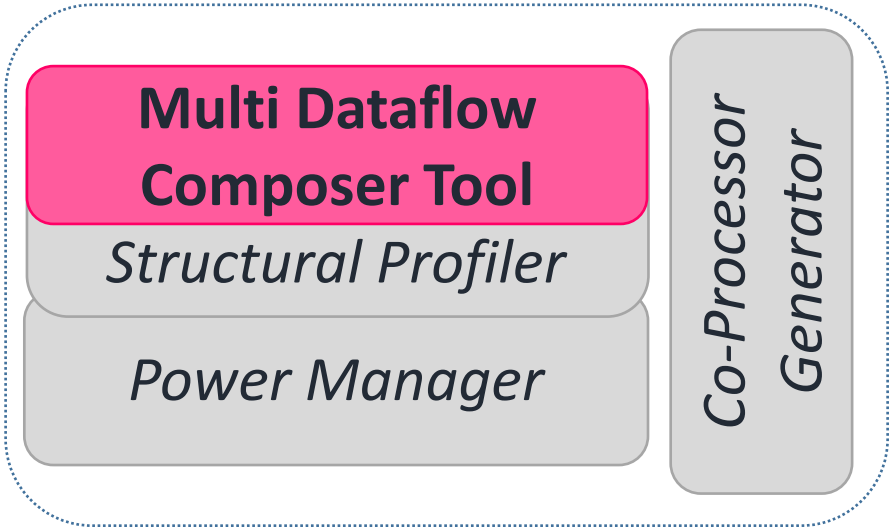

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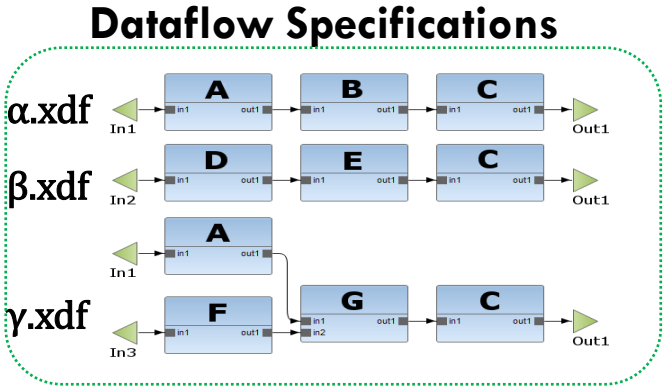

MDC tool: Dataflow to HW Mapping

Multi Dataflow Composer Tool

Structural Profiler

Power Manager

Co-Processor Generator

MDC design suite

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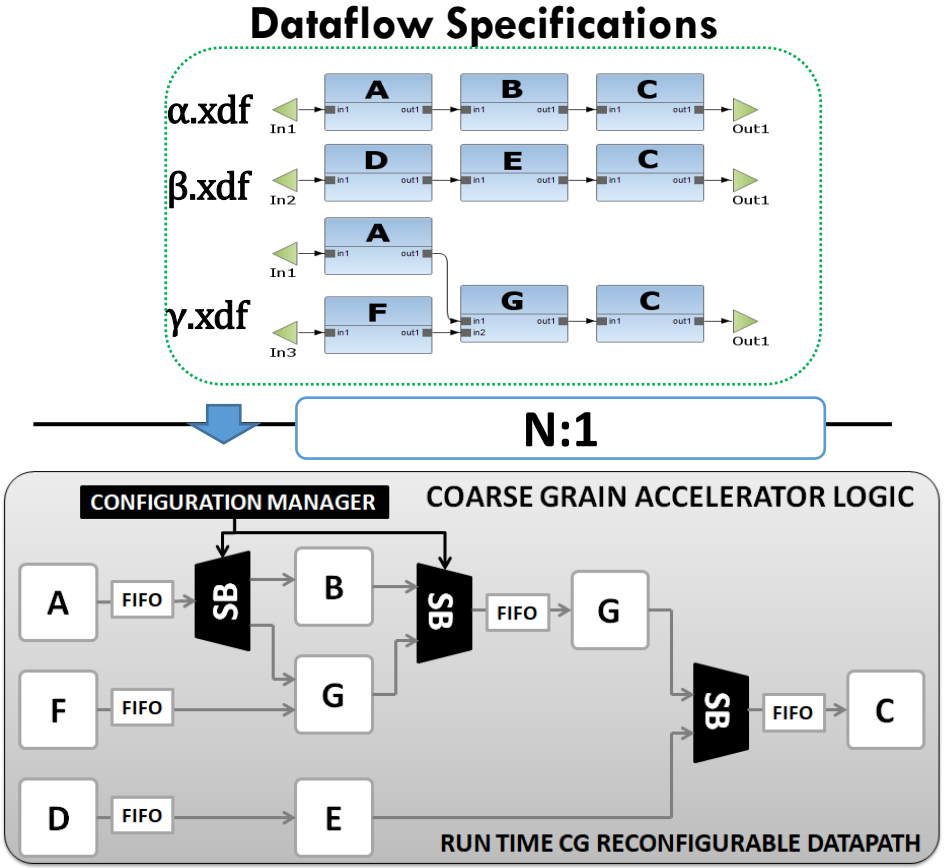
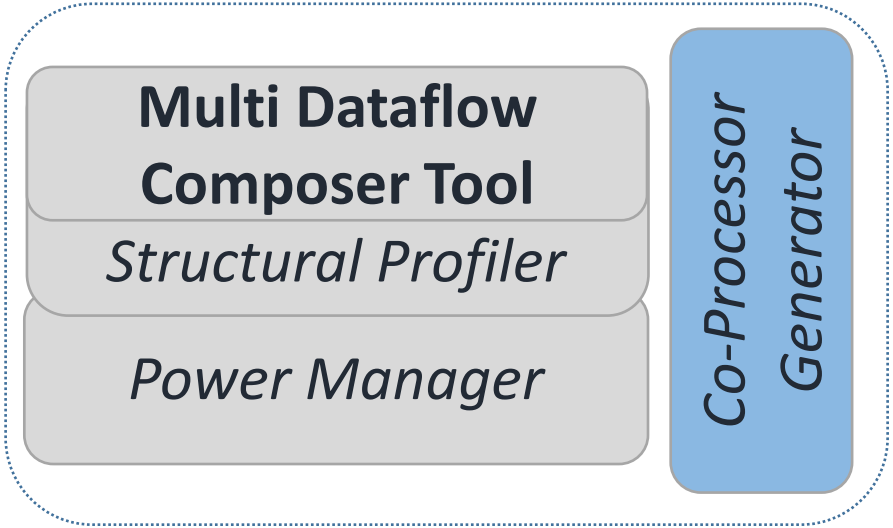


MDC Tool: Coprocessor Generator



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Co-Processor Generator:

generation of ready-to-use Xilinx IPs

MDC Tool: Coprocessor Generator

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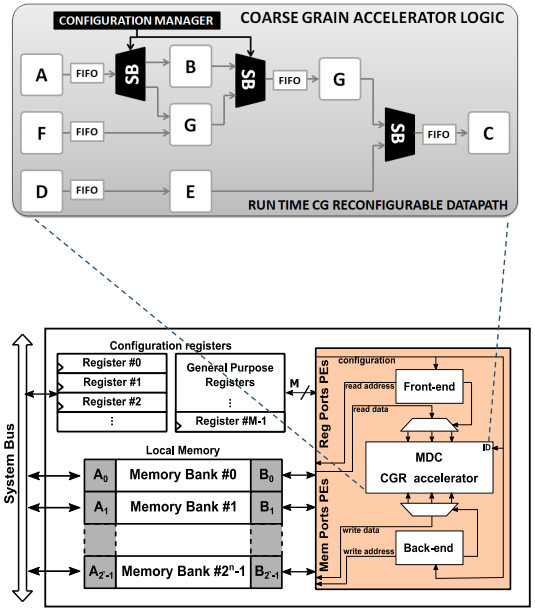
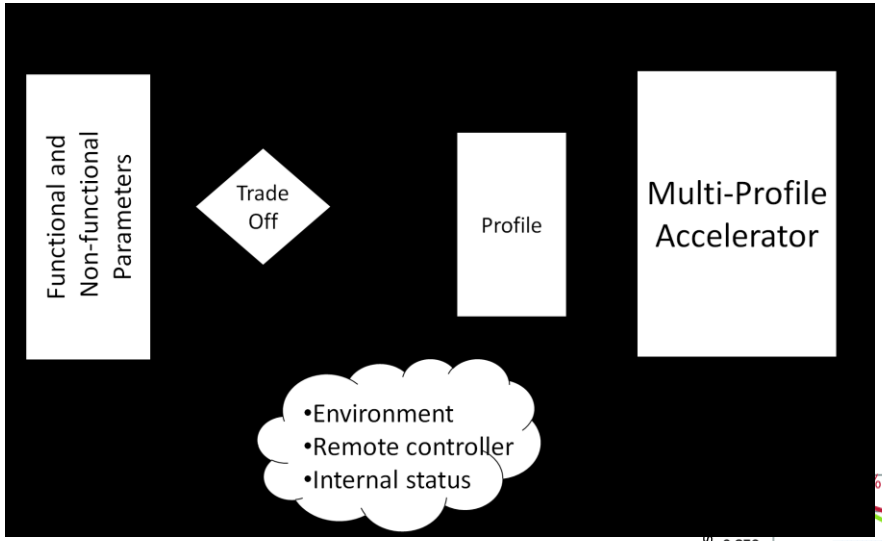
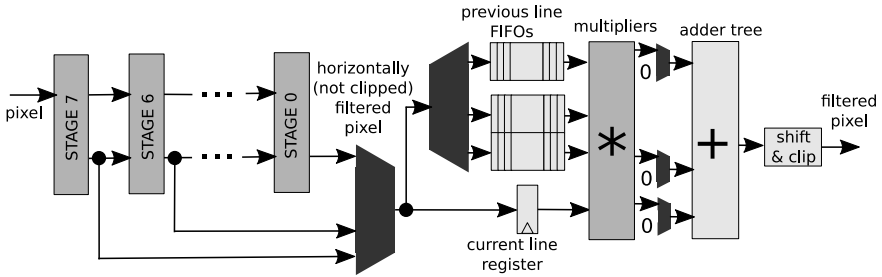
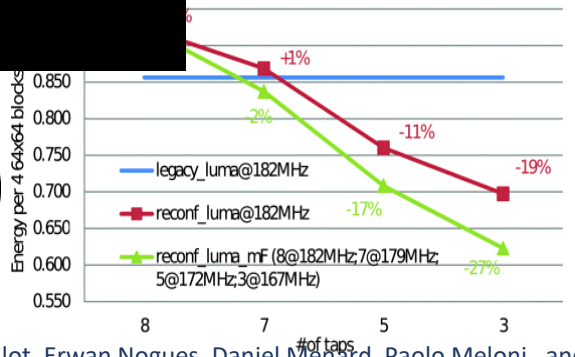


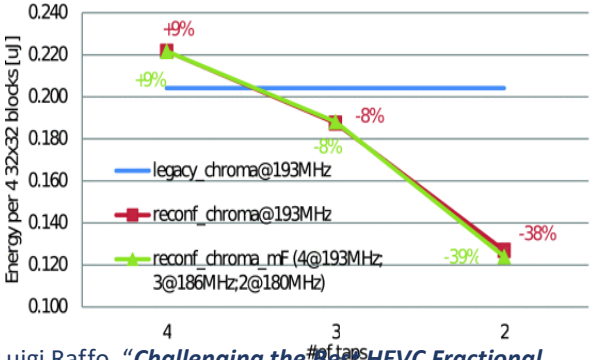
CG Reconfiguration: Runtime KPI Trade-Offs





Example of multi-profile CGR system: HEVC interpolator



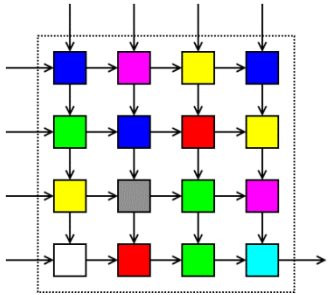


[ESL17] Carlo Sau, Francesca Palumbo, Maxime Pelcat, Julien Heulot, Erwan Nogues, Daniel Menard, Paolo Meloni, and Luigi Raffo. "***Challenging the Best HEVC Fractional Pixel FPGA Interpolators with Reconfigurable and Multi-frequency Approximate Computing***" in IEEE Embedded Systems Letters, vol. 9, no. 3, pp. 65-68, Sept. 2017.

DPR & CG-VRC

DPR → *Dynamic and Partial Reconfiguration*

- Lower reconfiguration speeds
- Better operation speed (no mux/less logic)
- Better Resource Utilization (no dark logic)
- Higher Flexibility and Scalability
- Technology dependent (FPGA)



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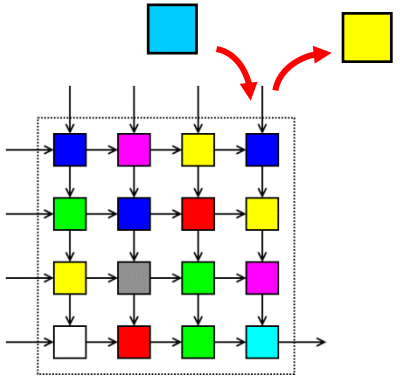

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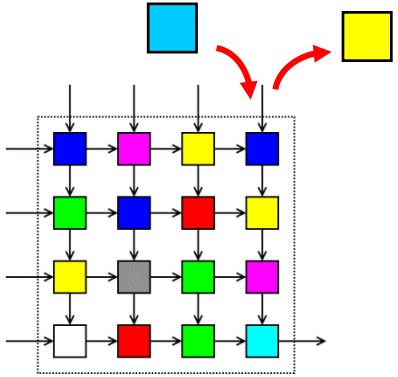

CG-VRC → *Coarse Grain - Virtual Reconfigurable Circuits*

DPR & CG-VRC

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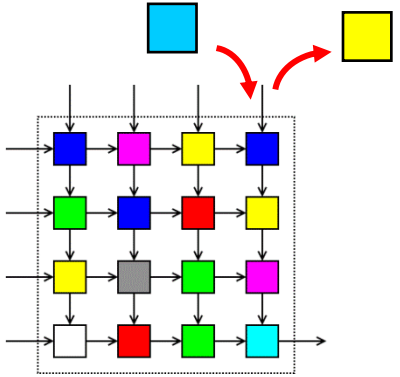
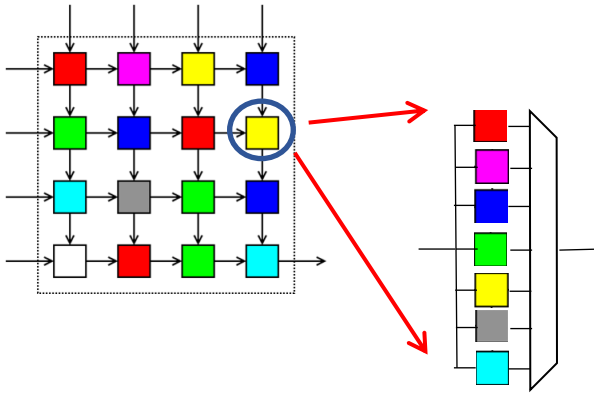


CG-VRC → *Coarse Grain - Virtual Reconfigurable Circuits*

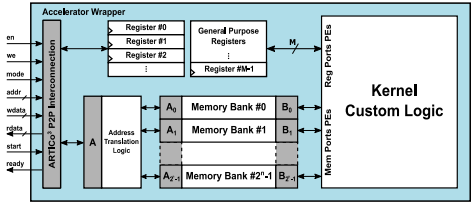
- High reconfiguration speed
- Lower operation speed (mux and size)
- Higher Area Overhead
- Technology independent (ASIC or FPGA)

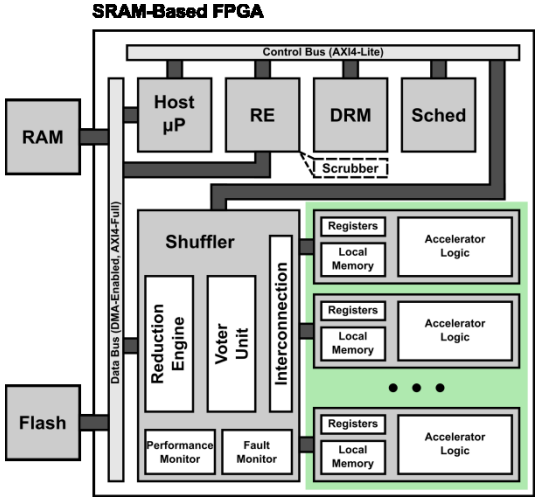


DPR + CG-VRC: ARTICo^3 + MDC

DPR + CG-VRC: ARTICo³ + MDC

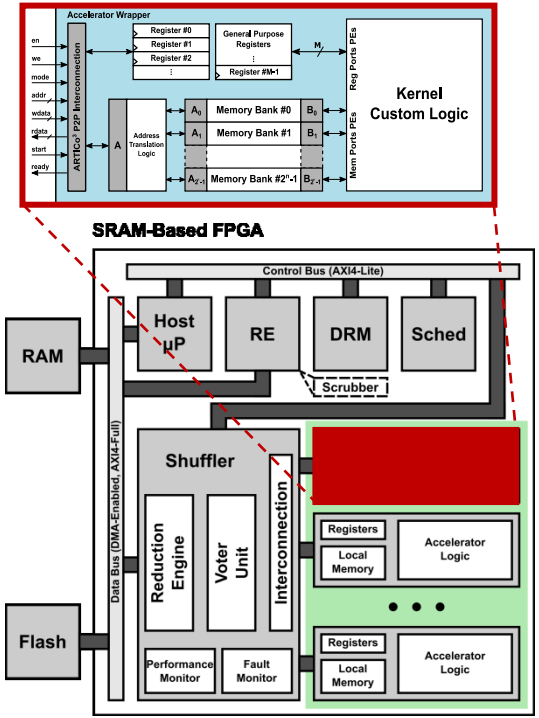
ARTICo3





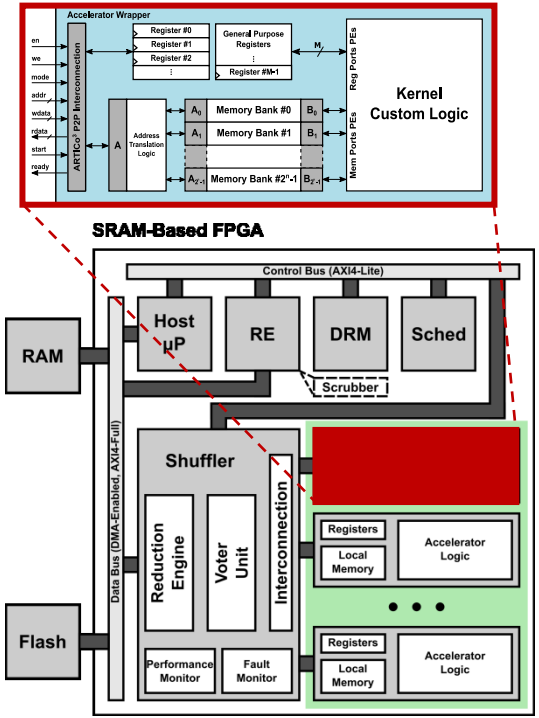
DPR + CG-VRC: ARTICo³ + MDC

ARTICo3

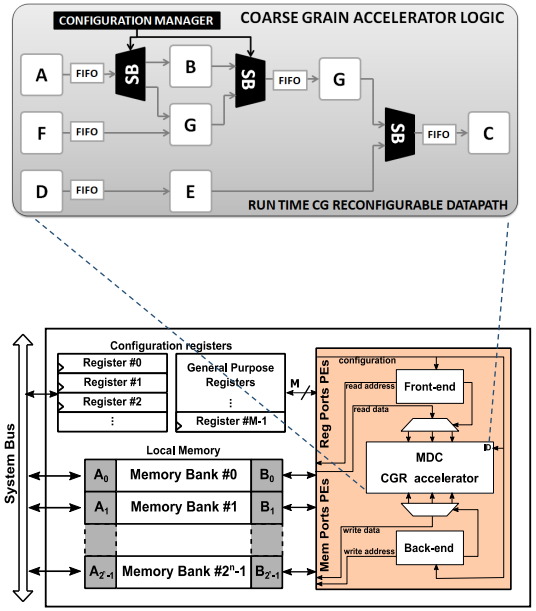


DPR + CG-VRC: ARTICo³ + MDC

ARTICo3

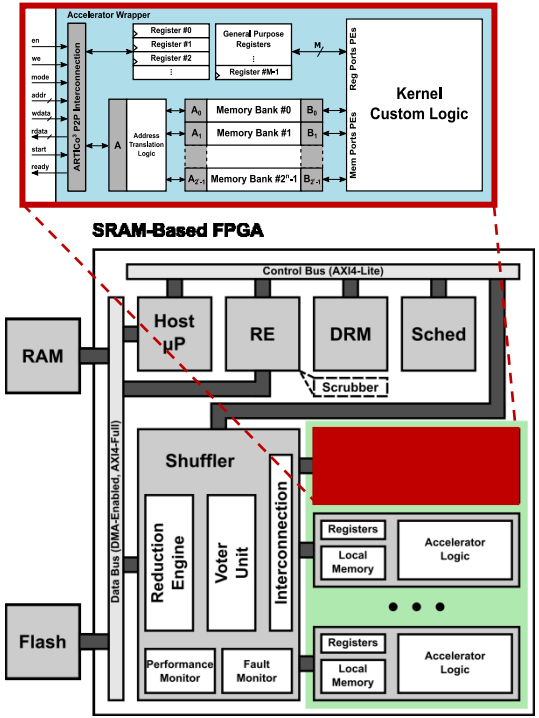


Coarse-Grain MDC Logic

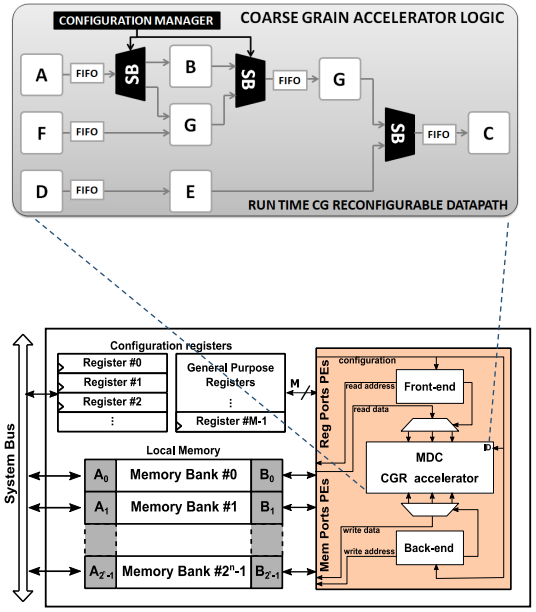


DPR + CG-VRC: ARTICo³ + MDC

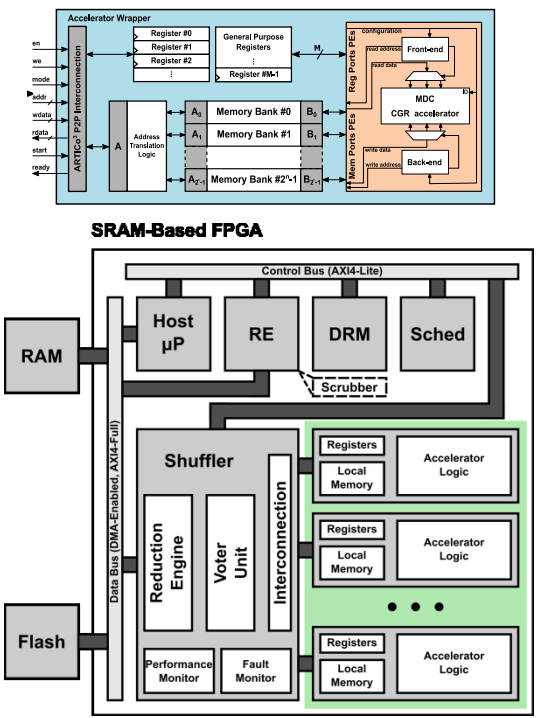
ARTICo3



Coarse-Grain MDC Logic

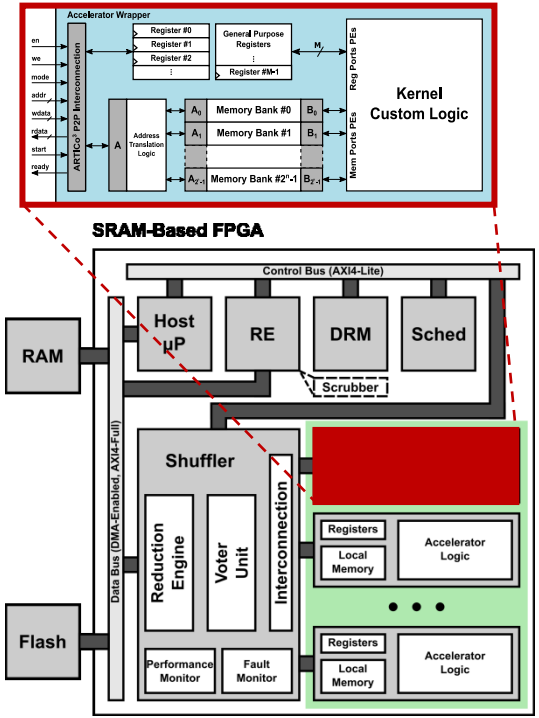


Mixed-Grain A3+MDC

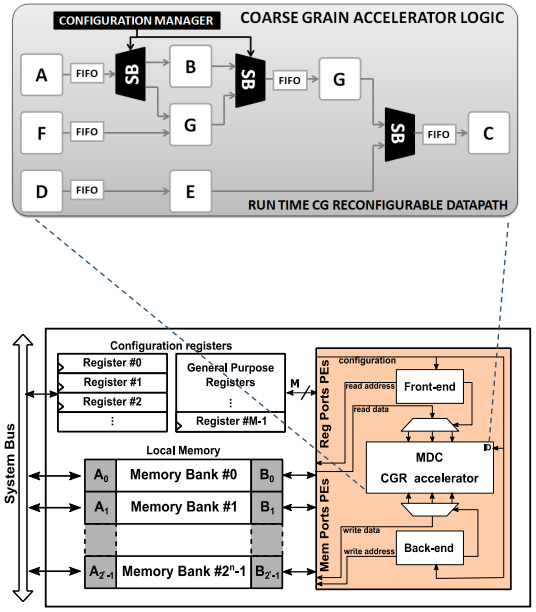


DPR + CG-VRC: ARTICo³ + MDC

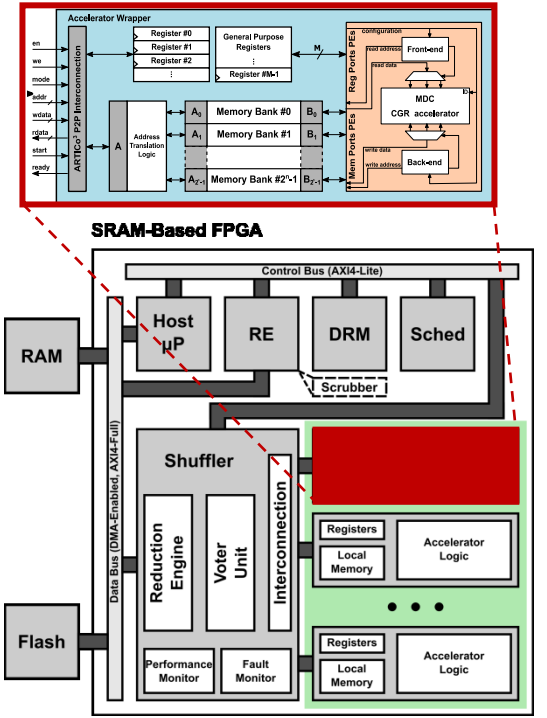
ARTICo3



Coarse-Grain MDC Logic



Mixed-Grain A3+MDC



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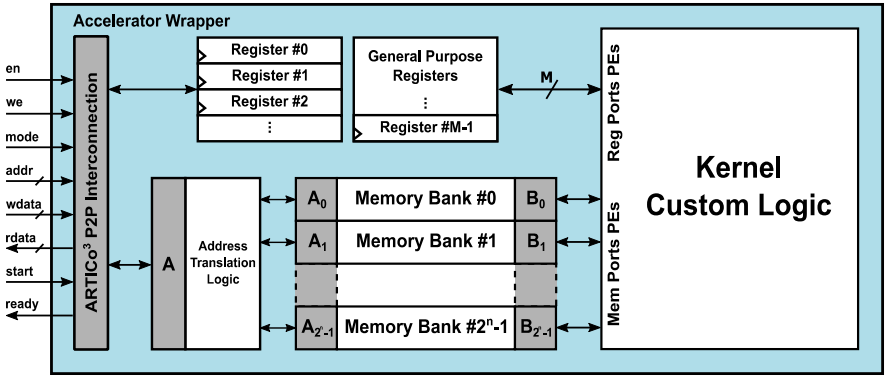
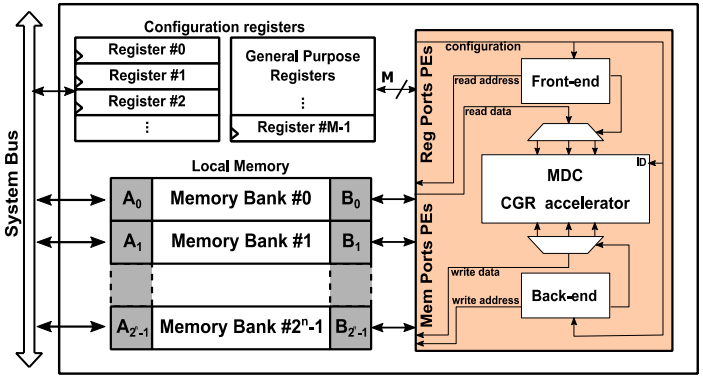
  - **ARTICo3 + MDC integration**
- Next-steps
  - Monitoring
  - Adaptivity Support

ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper

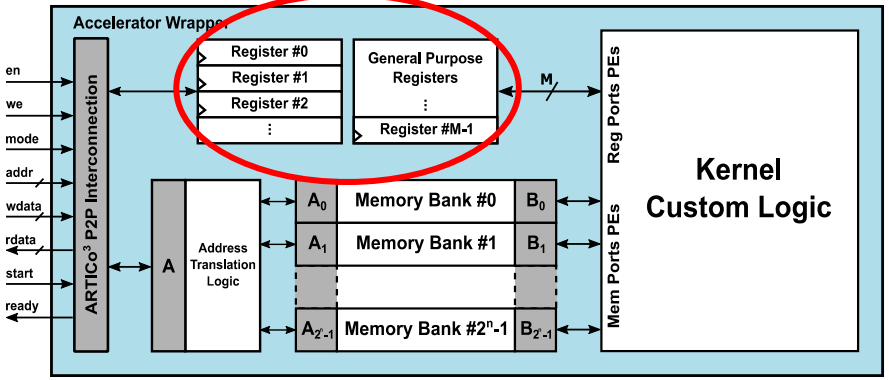


MDC generated IP



ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper



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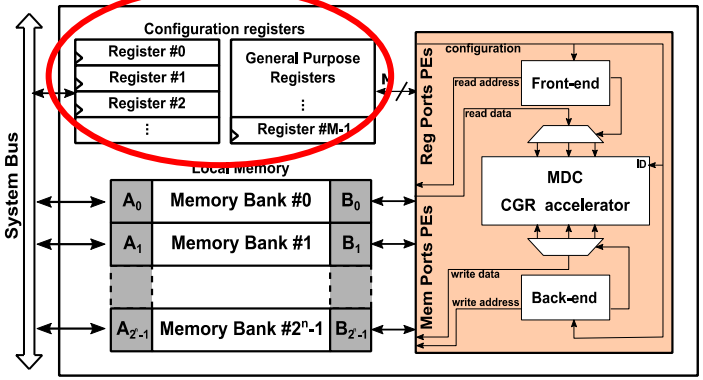
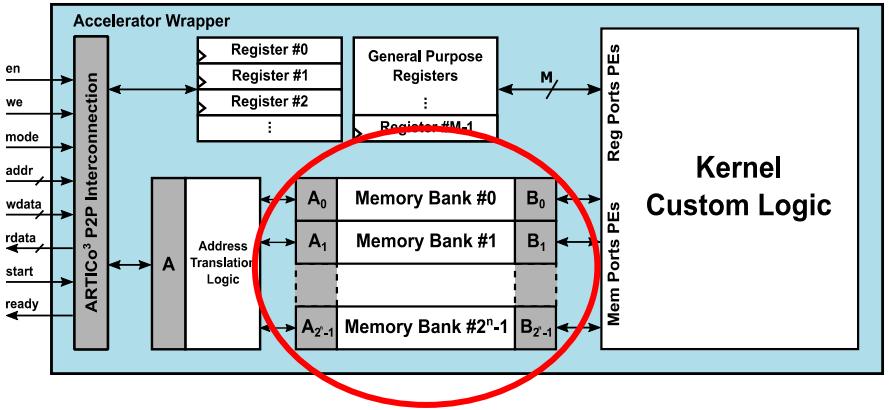


ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper



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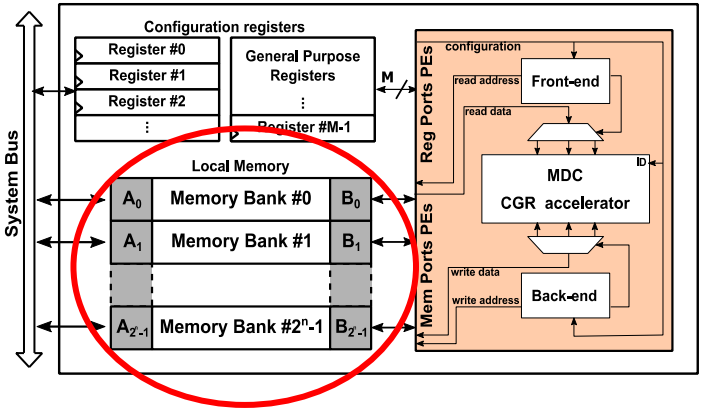
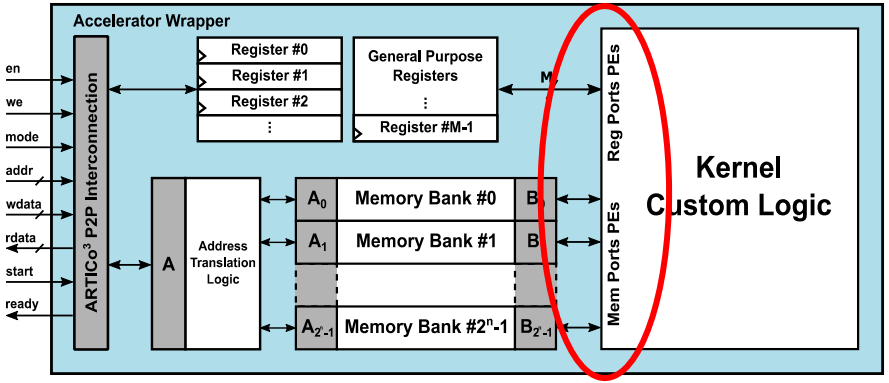


ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper



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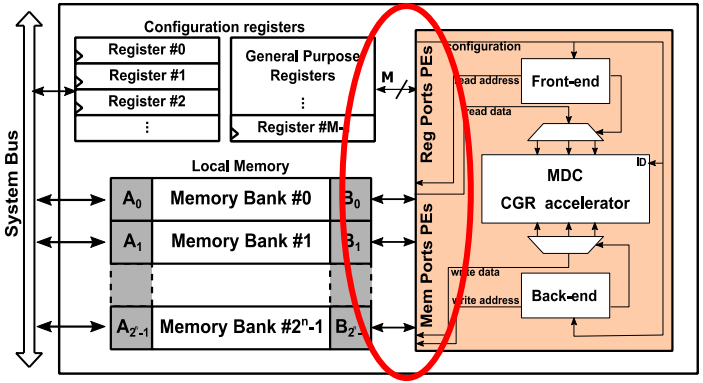
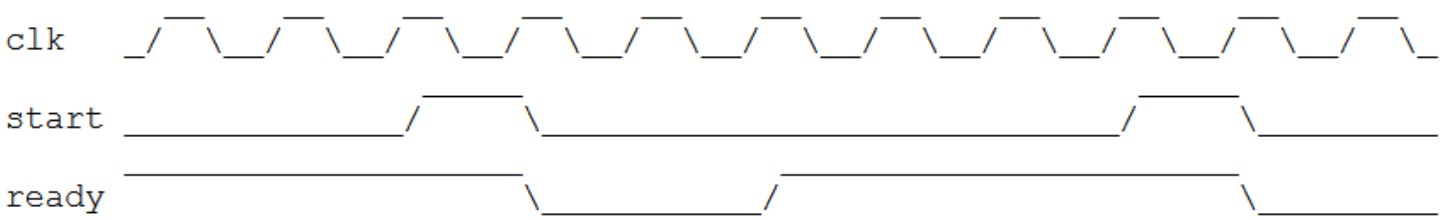
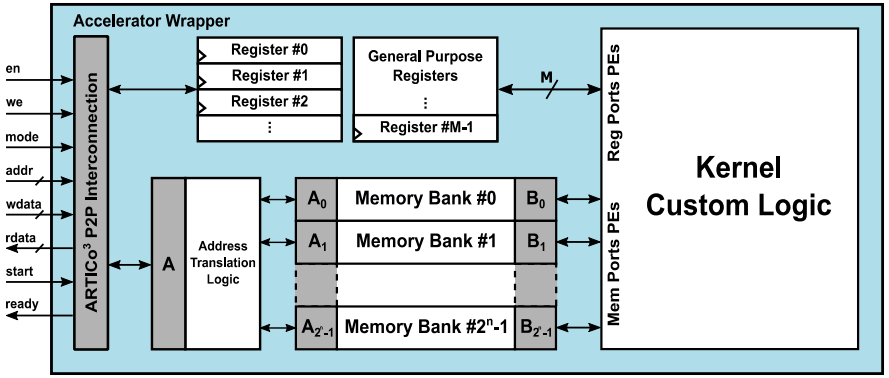




ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper



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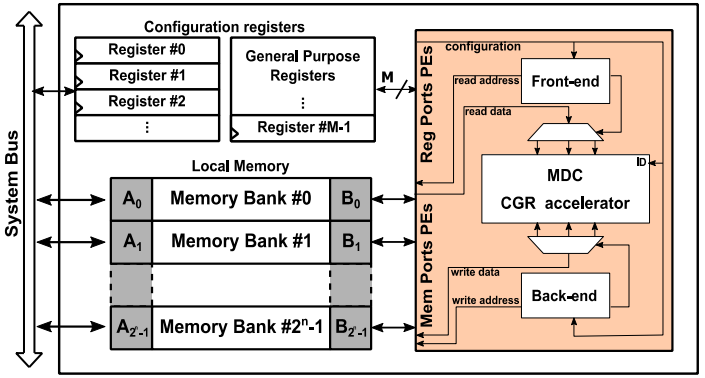
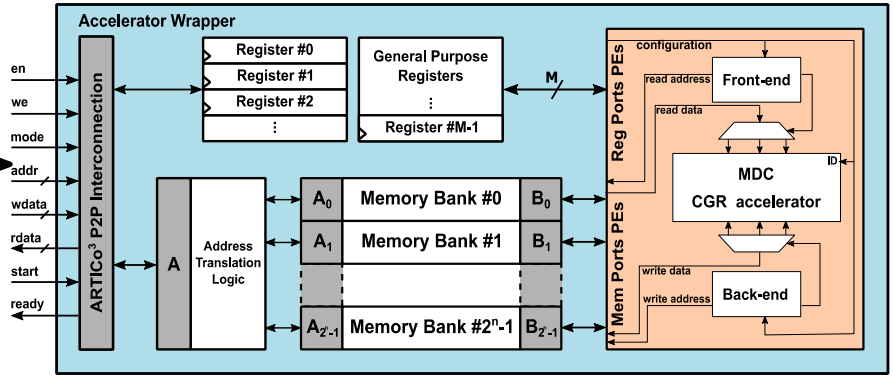
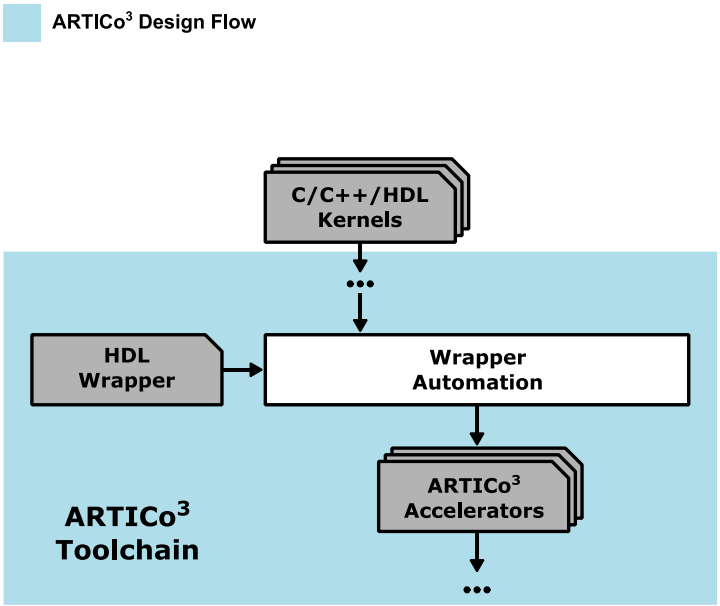
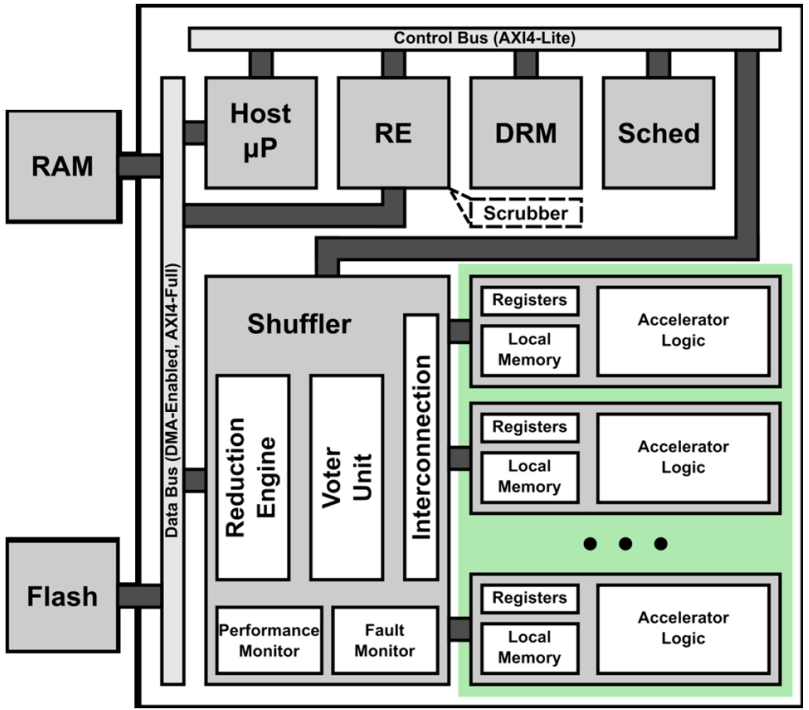




ARTICo³ + MDC: Integration

Hardware Design Flow

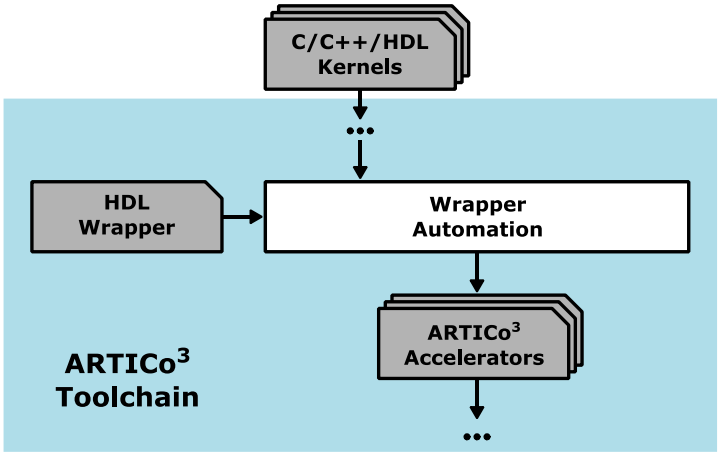


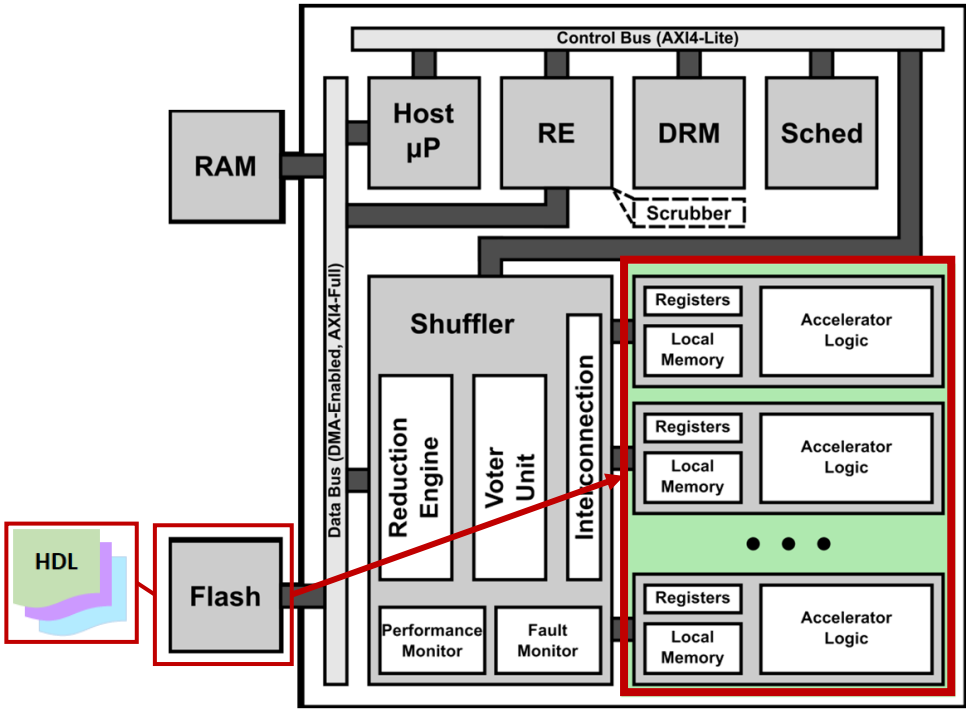


ARTICo³ + MDC: Integration

Hardware Design Flow

ARTICo³ Design Flow





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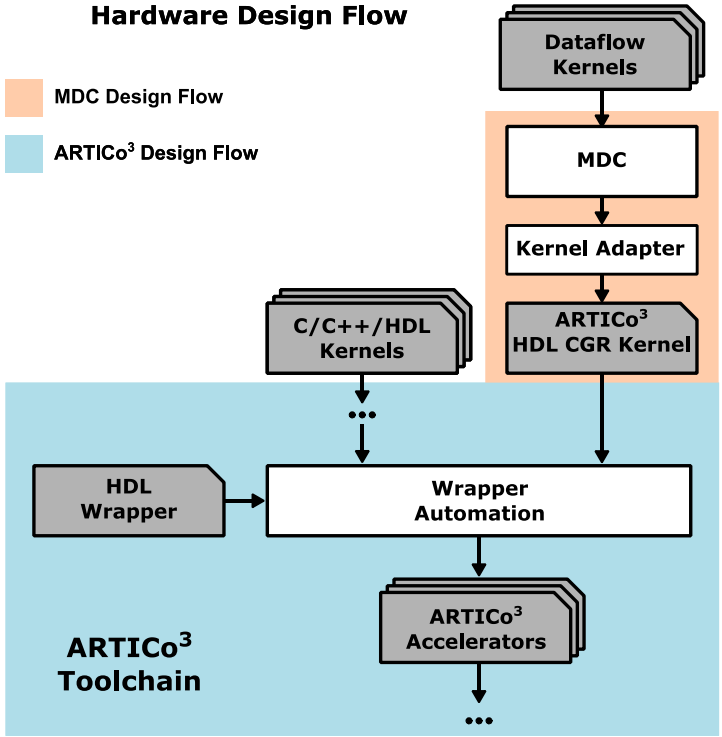

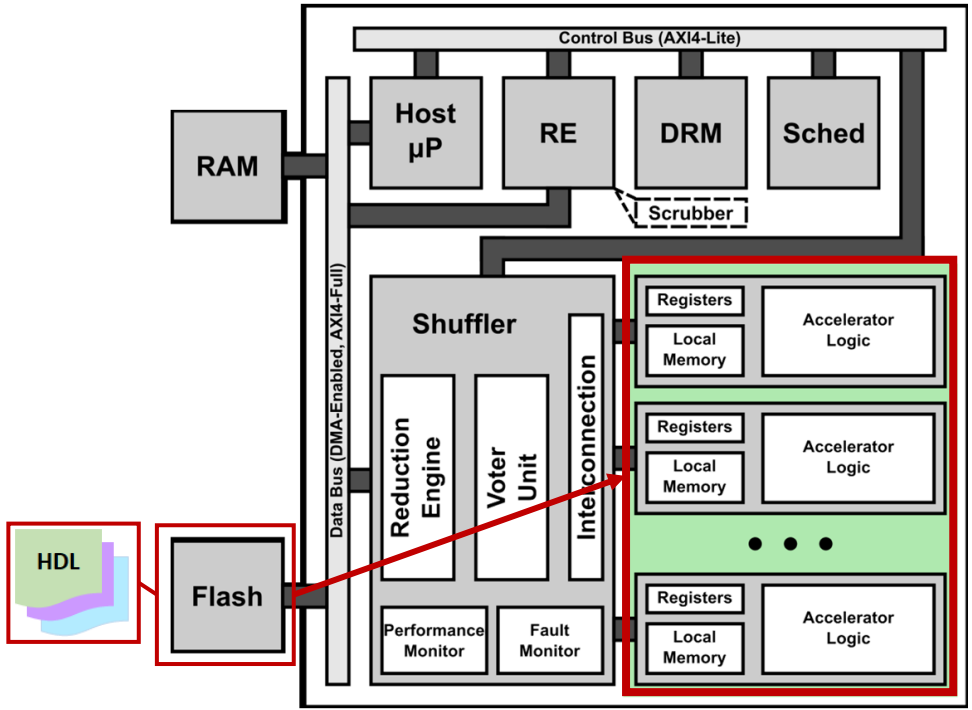

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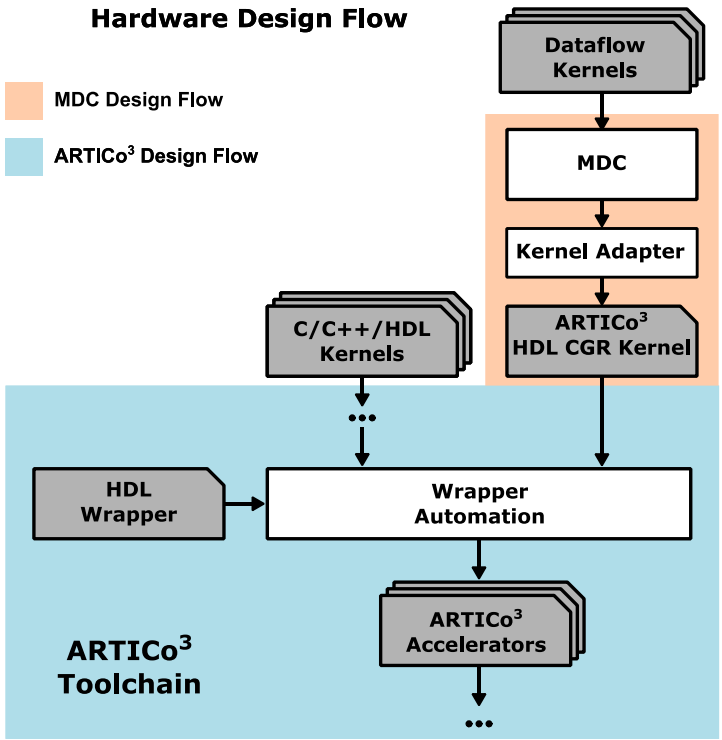
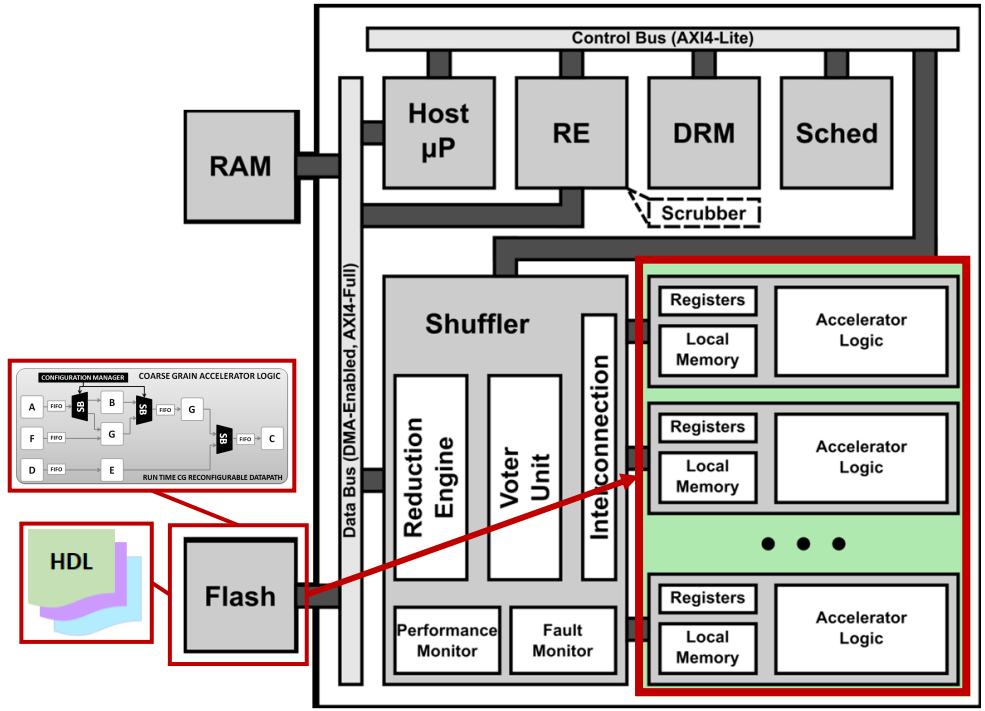
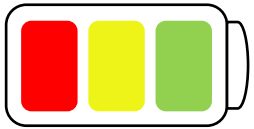
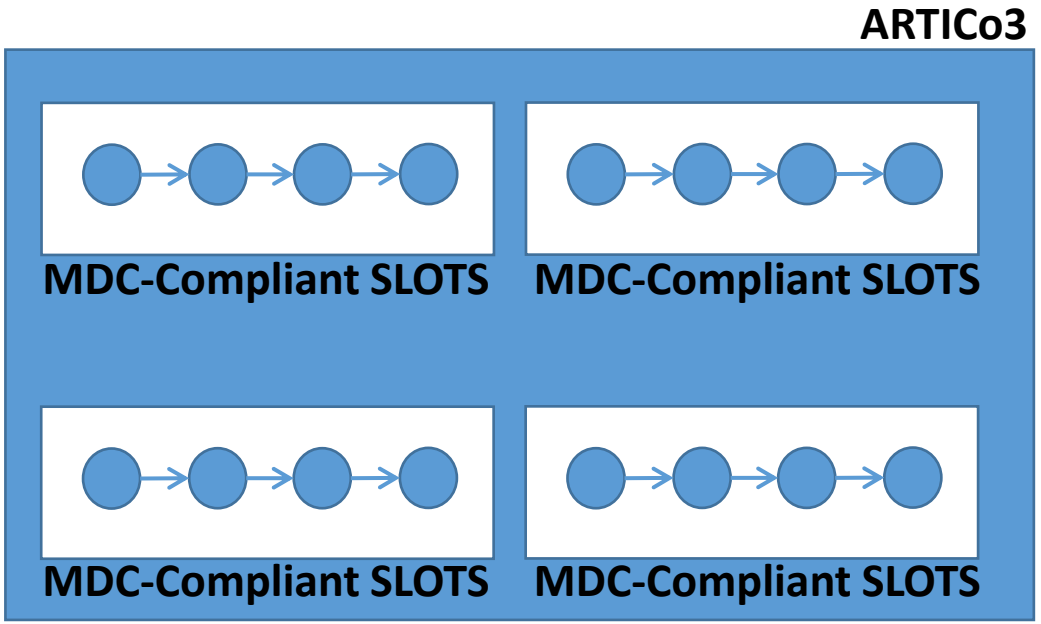




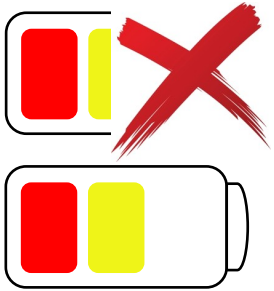
ARTICo³ + MDC: Mixed-Grain



Max Troughput
Max QoS

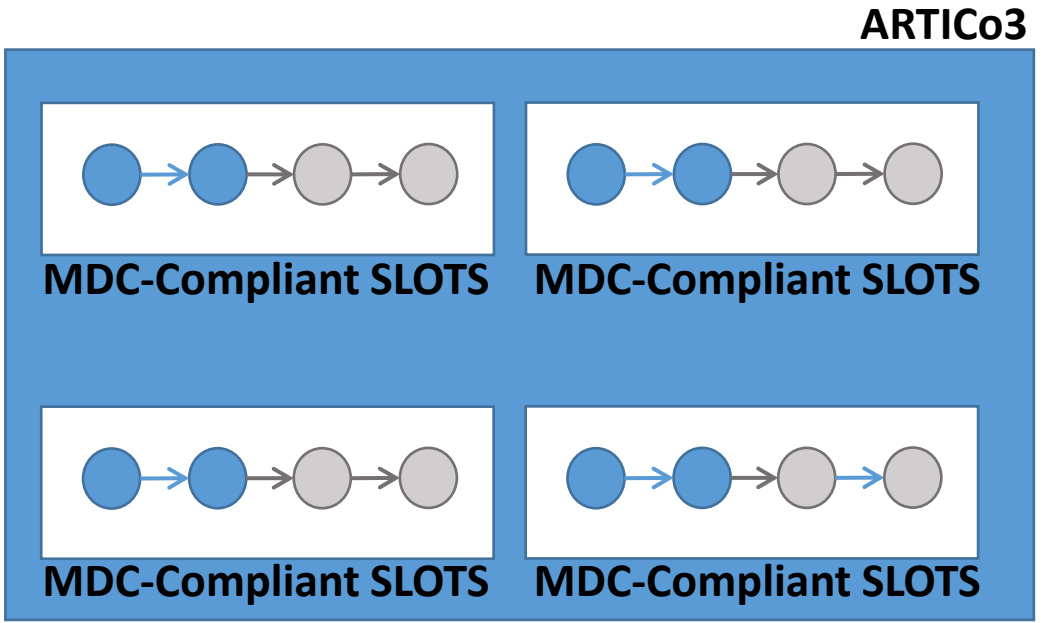


ARTICo³ + MDC: Mixed-Grain

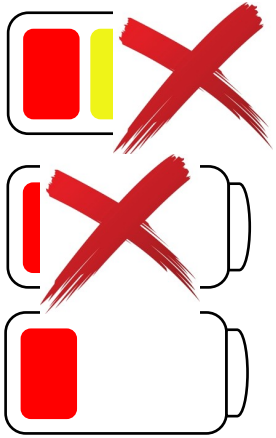


Max Troughput
Max QoS

Max Troughput
Degraded QoS



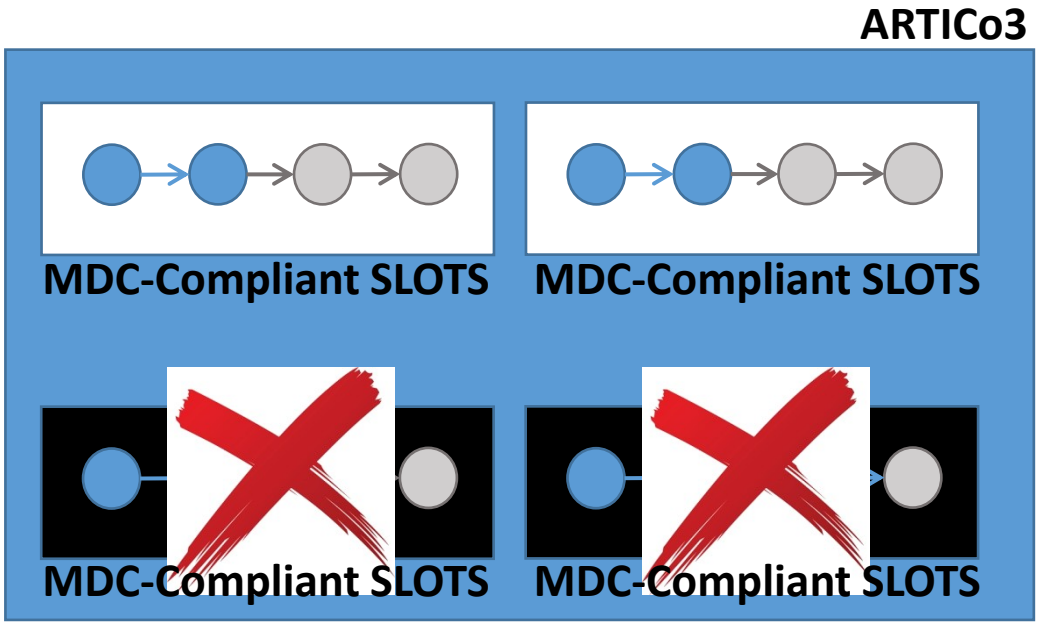
ARTICo³ + MDC: Mixed-Grain



Max Troughput
Max QoS

Max Troughput
Degraded QoS

Less Troughput
Degraded QoS



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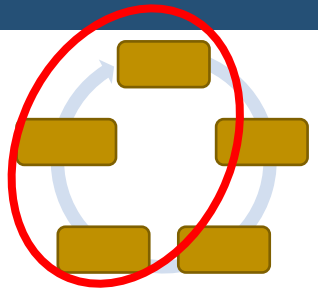
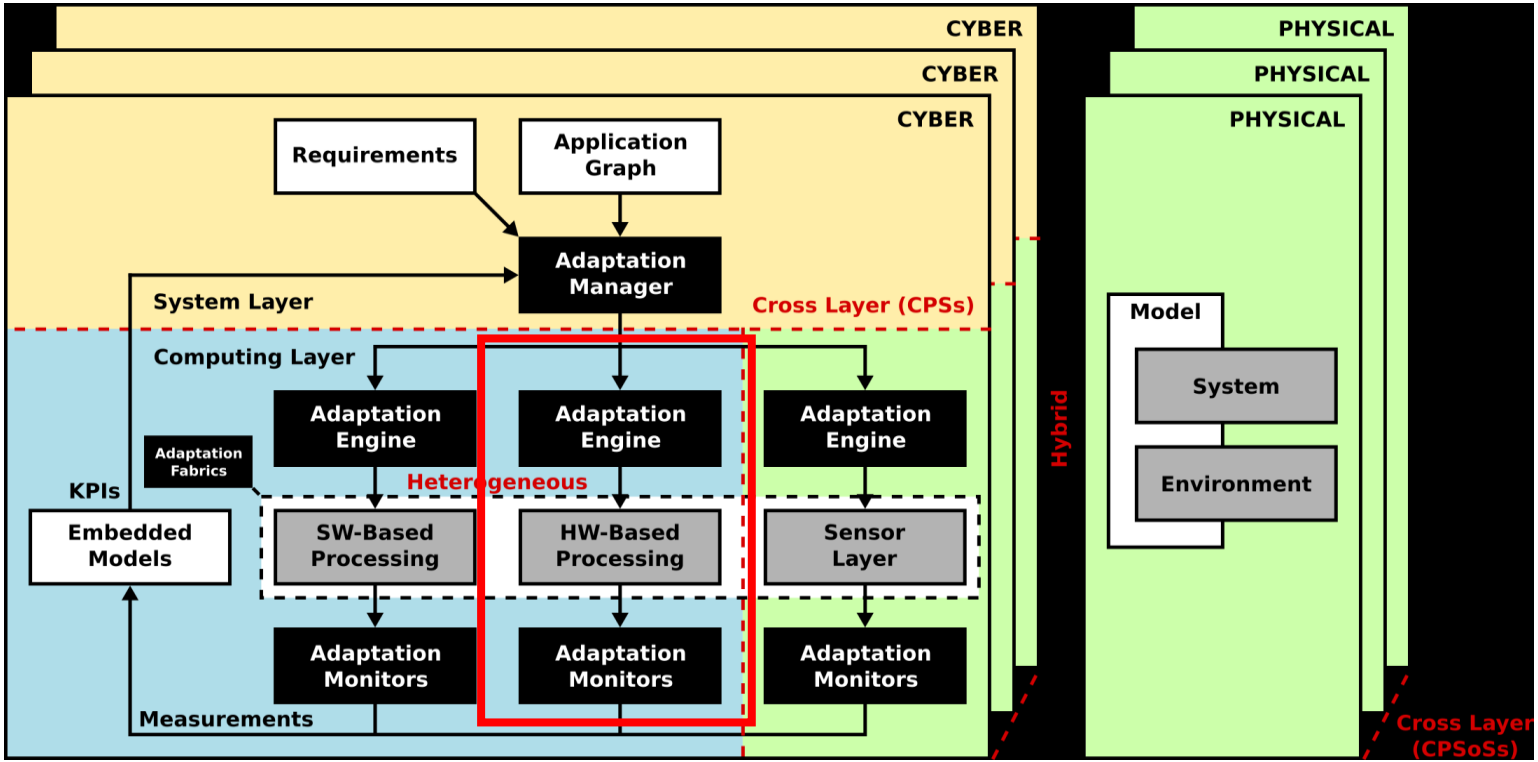
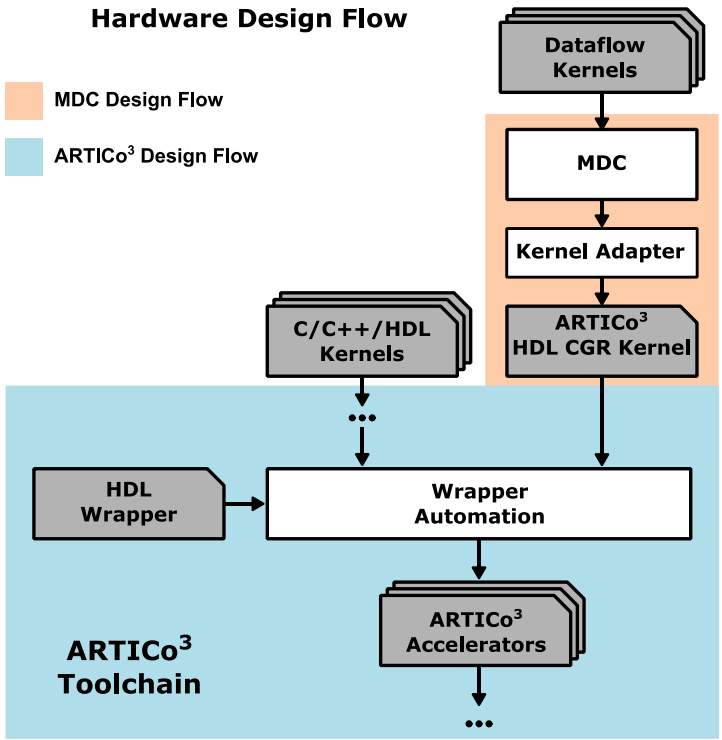
  - **Adaptivity Support**

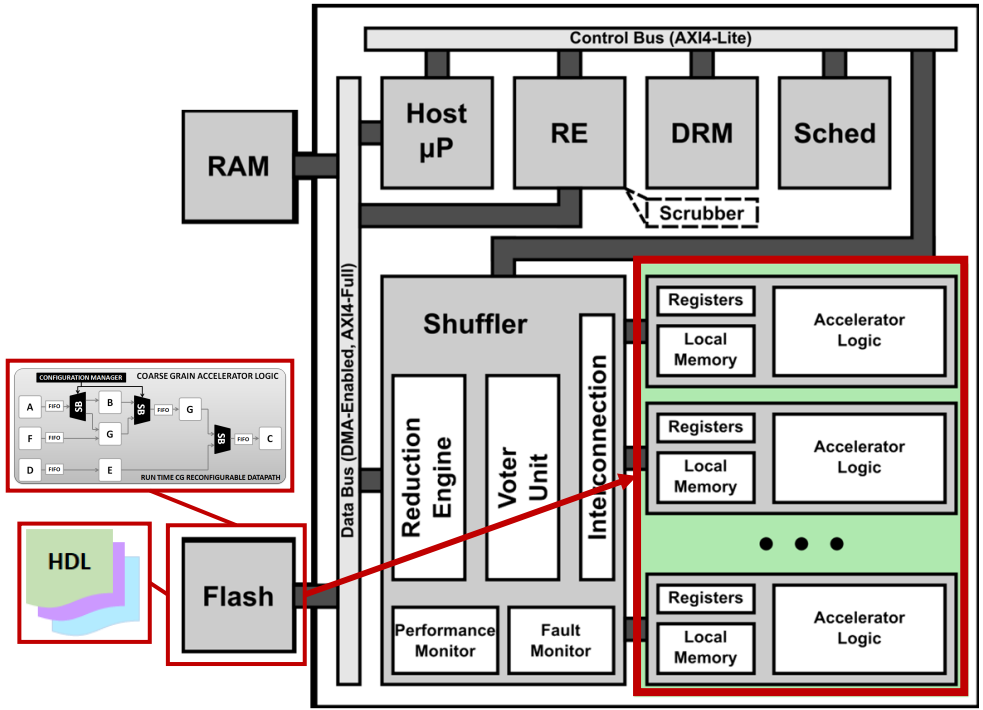
Self-Adaptation in CERBERO H2020: Monitors



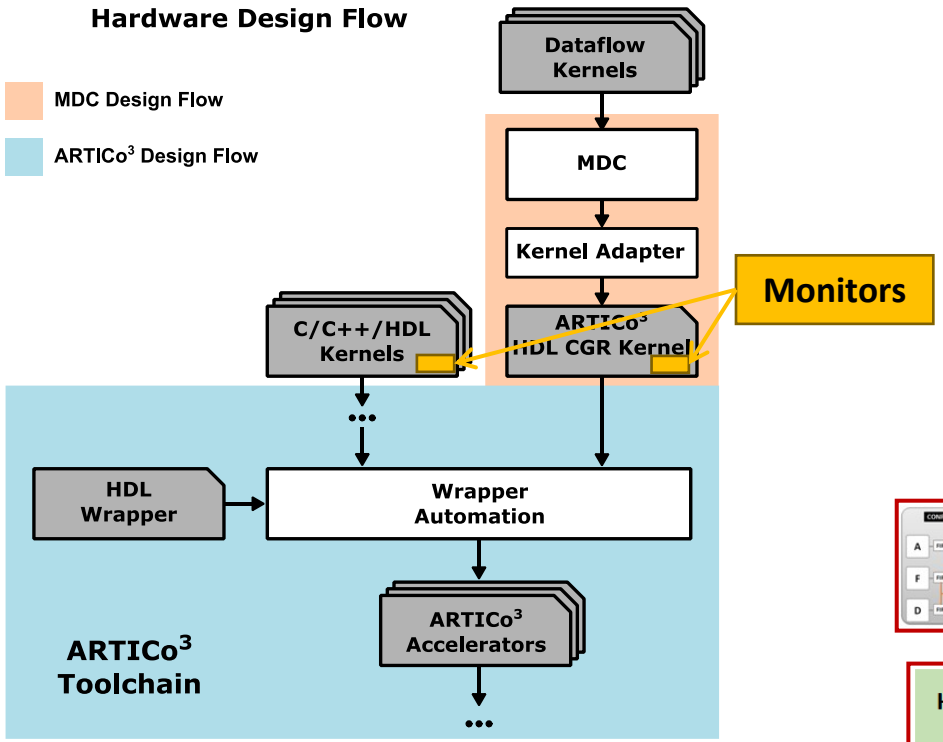


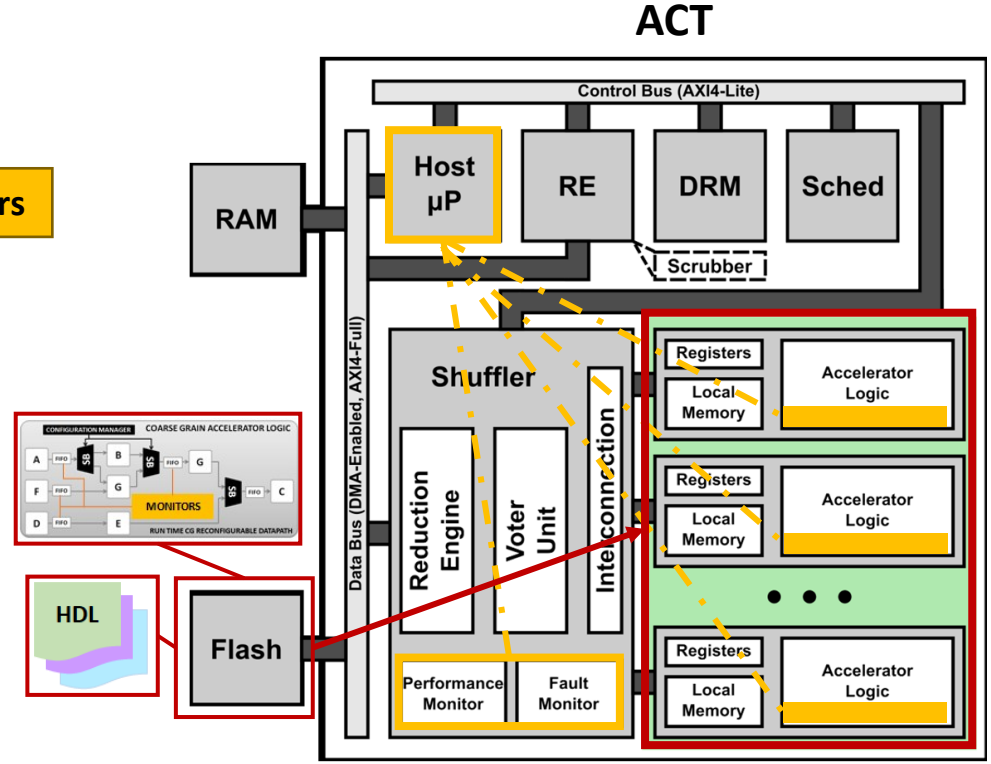
Mixed-Grain Adaptivity





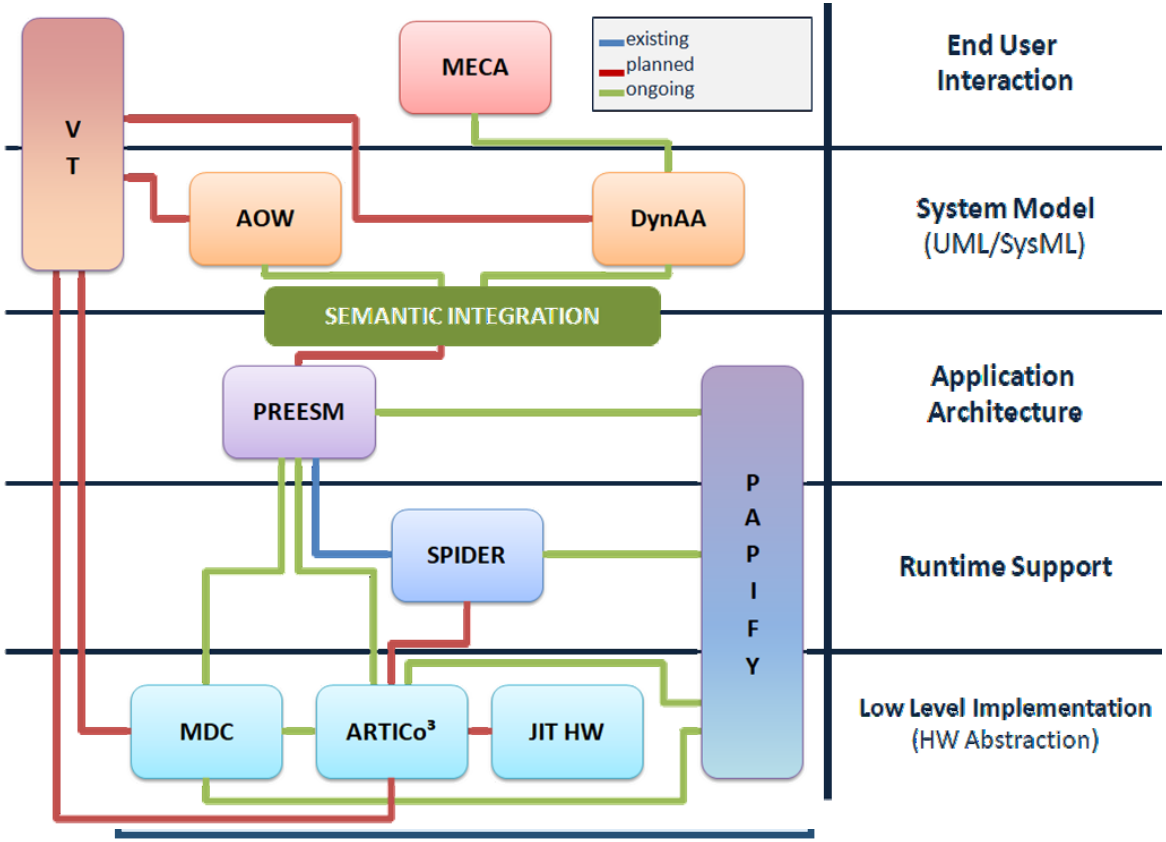
Mixed-Grain Self-Adaptivity



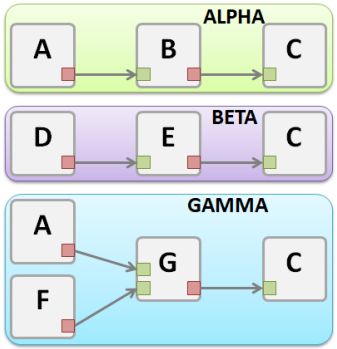


Adaptivity Support: CERBERO Framework

- CERBERO Framework
  - Integrated design environment to ***model, explore, deploy and verify*** complex ***adaptive CPS***
  - Address the lack of integrated toolchains capable of:
    - Spanning across layers
    - ***Dealing with adaptivity and heterogeneity***
    - Providing system in the loop co-simulation



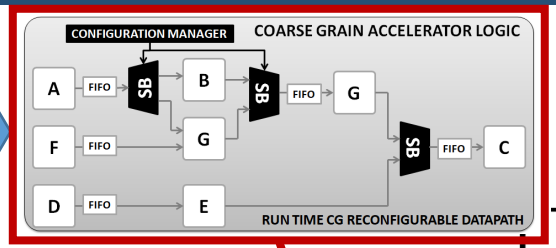
Adaptivity Support @ Design-Time



N

PREESM
+
MDC

1



Partitioning
+ CGR Accelerator Synthesis

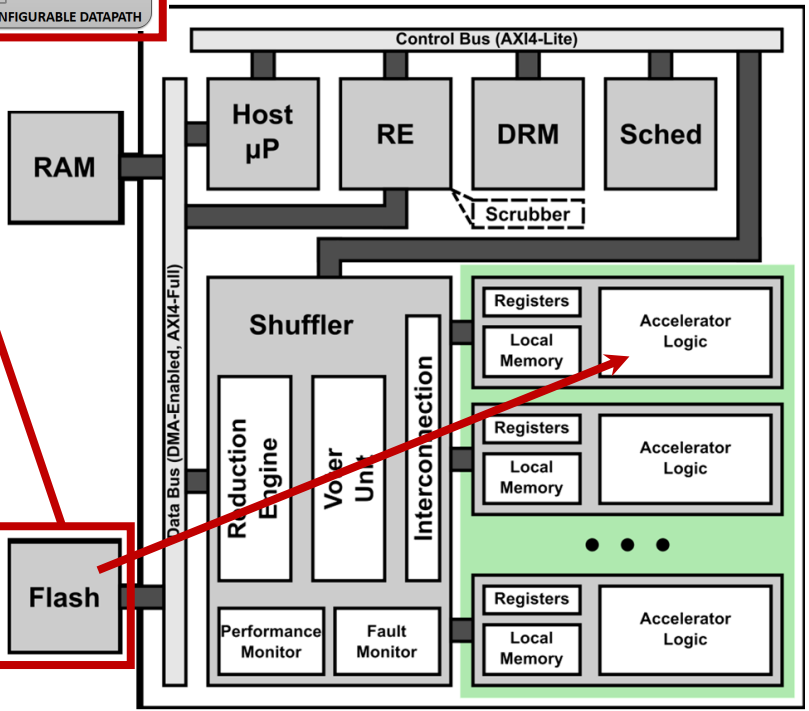
N

PREESM
+
SDSoC

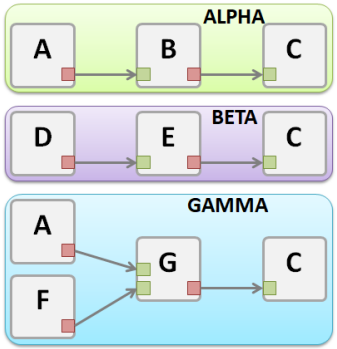
N

HDL

Partitioning
+
Slots Synthesis



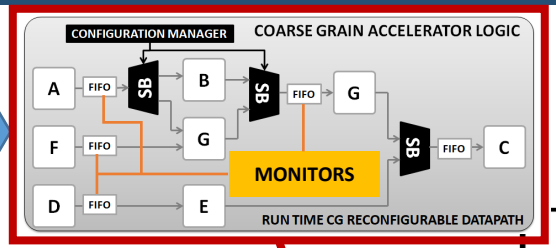
Adaptivity Support @ Run-Time



N

PREESM
+
MDC
+
PAPI

1



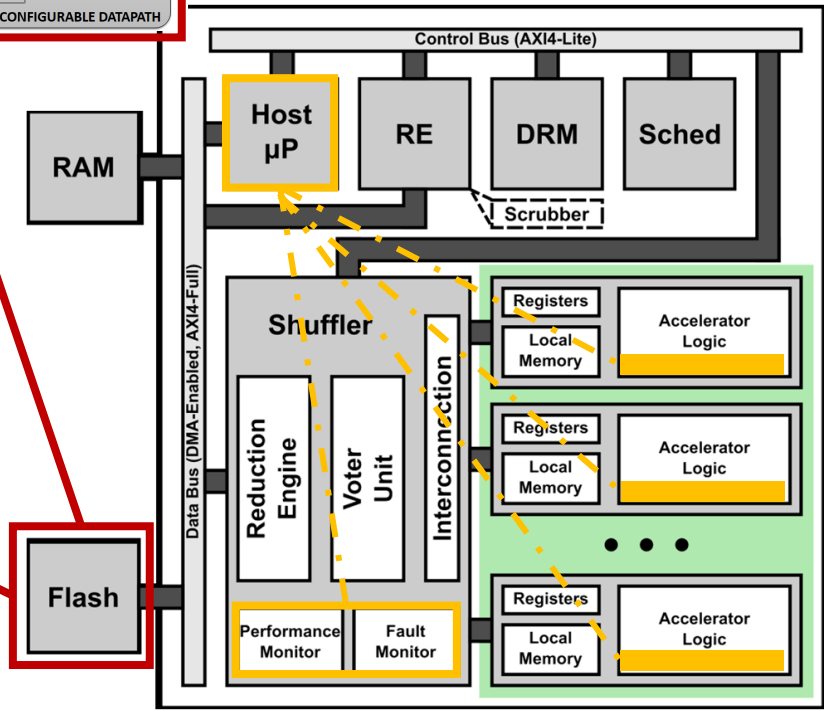
N

PREESM
+
SDSoC
+
PAPI

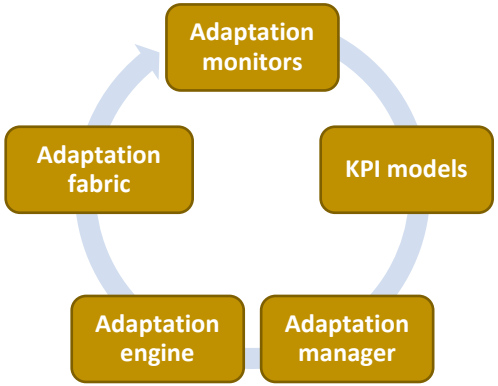
N

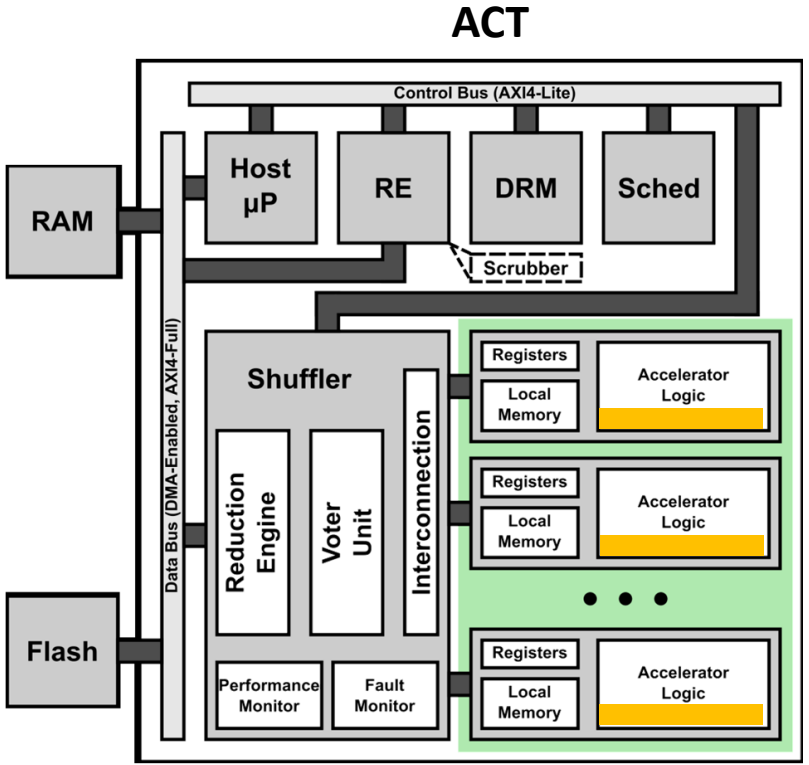
HDL

Runtime Performance Monitoring

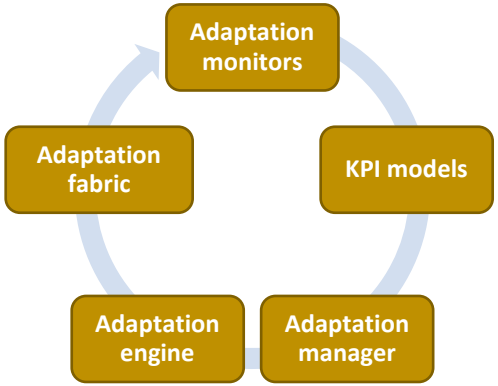


HW Adaptation Loop: CERBERO Tools





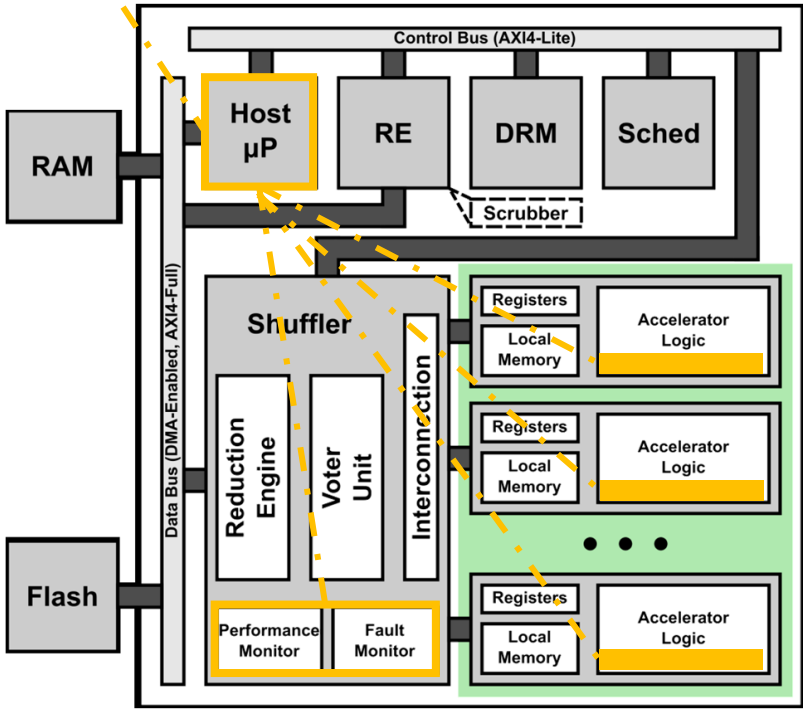
HW Adaptation Loop: CERBERO Tools



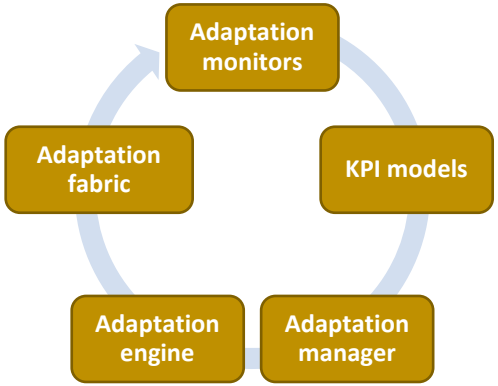
PAPI

MONITOR

ACT



HW Adaptation Loop: CERBERO Tools



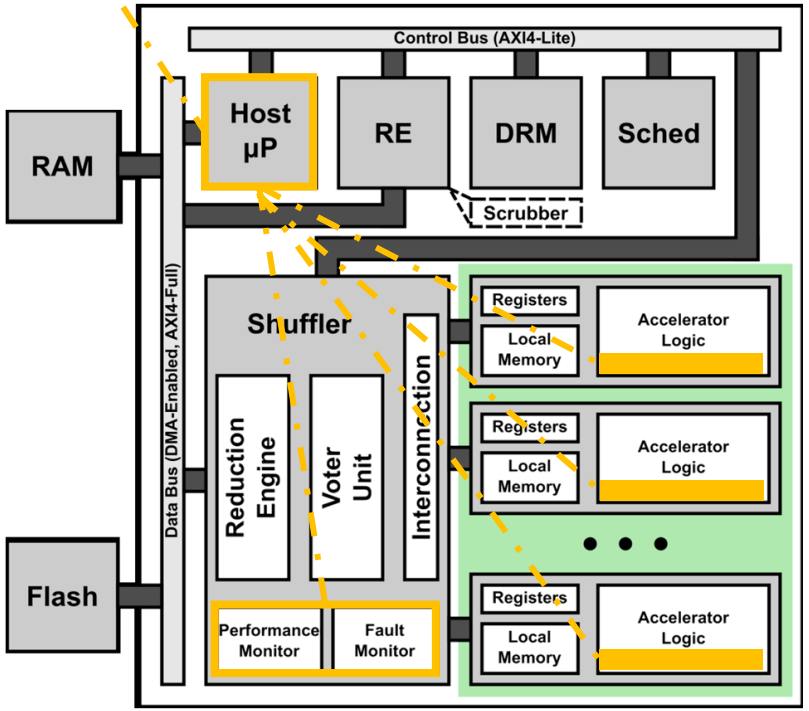
PAPI

MONITOR

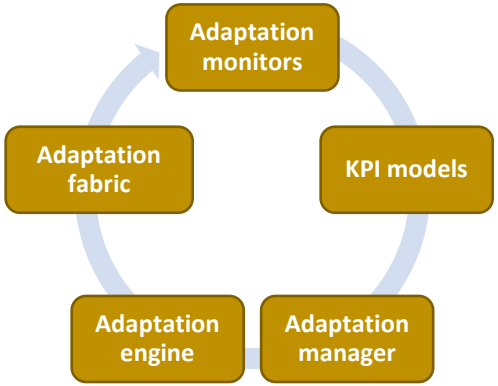
INFORM

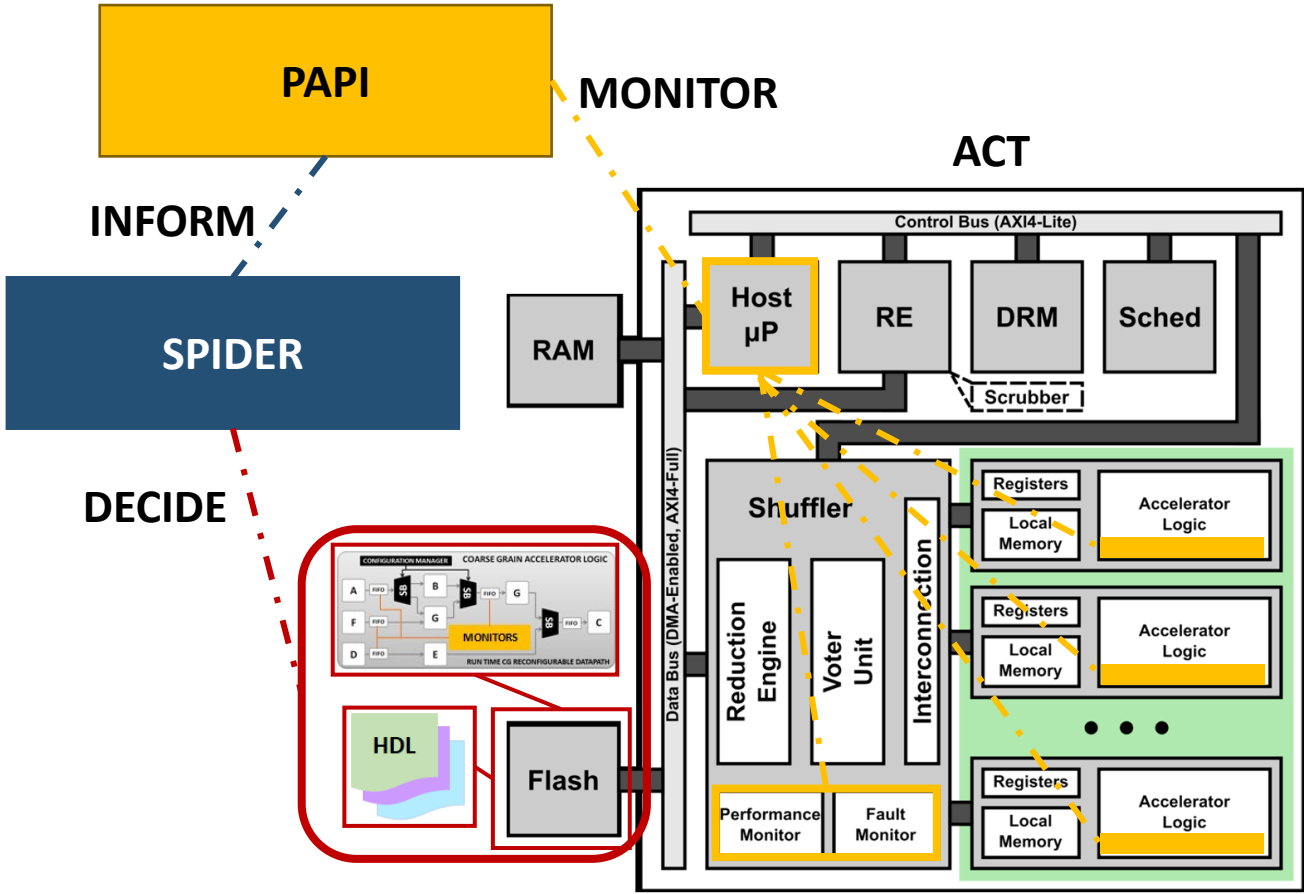
SPIDER

ACT

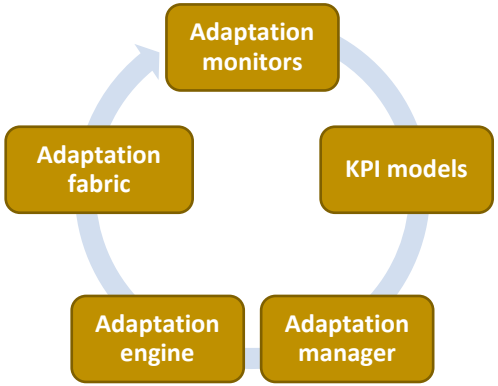


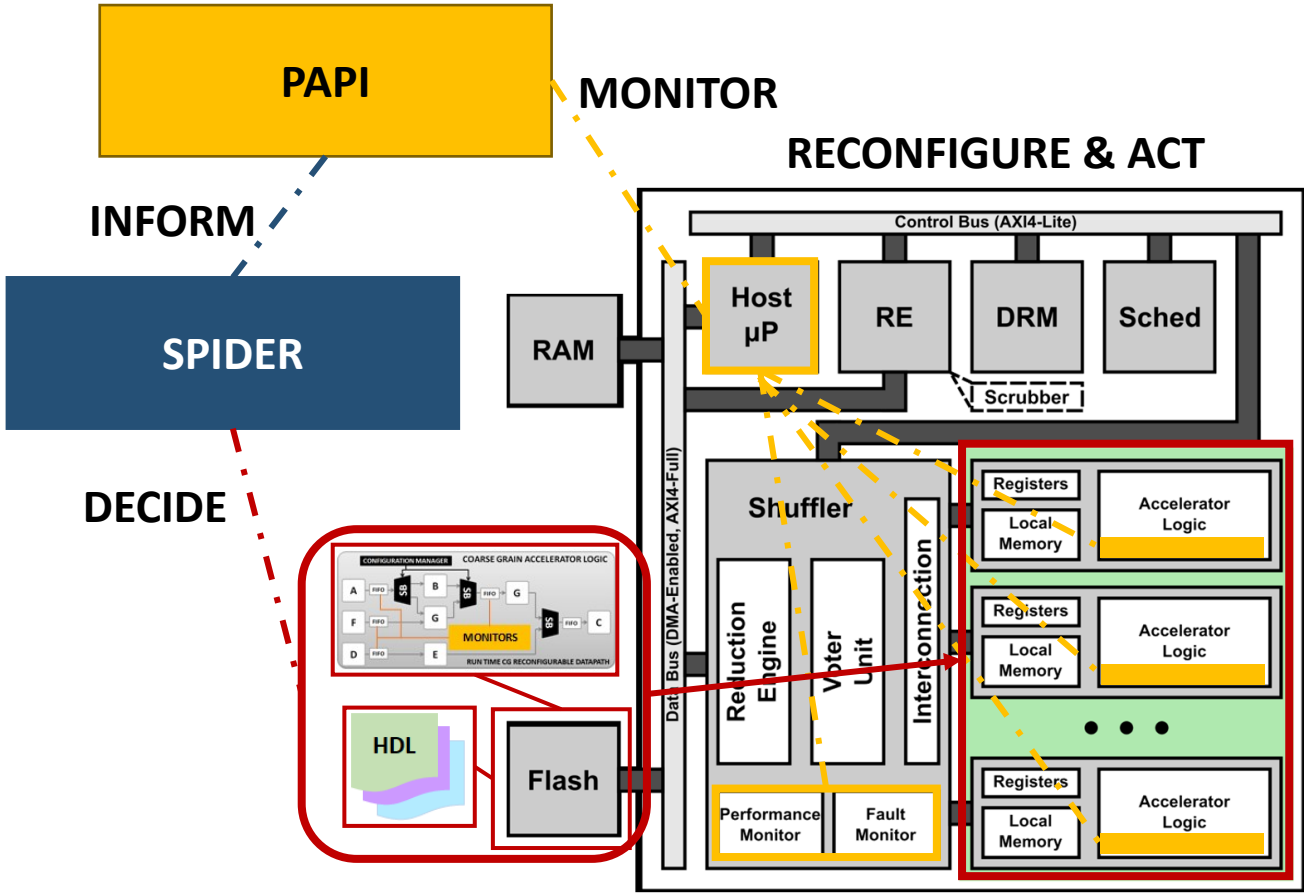
HW Adaptation Loop: CERBERO Tools





HW Adaptation Loop: CERBERO Tools





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CERBERO

Thank you for your attention

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