INSA

The Future Directions of Dataflow-Based Reconfigurable Hardware Accelerators

Francesca Palumbo[1], Claudio Rubattu[1,2], **Carlo Sau**[3], Tiziana Fanni[3], Luigi Raffo[3]

[1]University of Sassari, PolComIng – Information Engineering Group

[2]University of Rennes, INSA Group

[3]University of Cagliari, Diee – Microelectronics and Bioengineering Group

Rennes, 12-14 December 2017

Outline

- MDC Tool Summary
  - Motivation and Approach
  - Current Functionalities and Future Directions
- Hardware-Software Partitioning
  - Co-Processing Support and Automated Characterization
- Enhancing the MDC High-Level Synthesis Support
  - Integration with the CAPH HLS engine
- Run-time Monitoring of CGR Accelerators
  - Extension of PAPI for dataflow in CGR hardware
- Providing Further Degrees of Reconfigurability
  - Mixed-Grain Reconfiguration Possibilities

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MDC tool Summary

Motivations

HIGH PERFORMANCES

real time, portability, long battery life

UP-TO-DATE SOLUTIONS

last audio/video codecs, file formats...

MORE INTEGRATED FEATURES

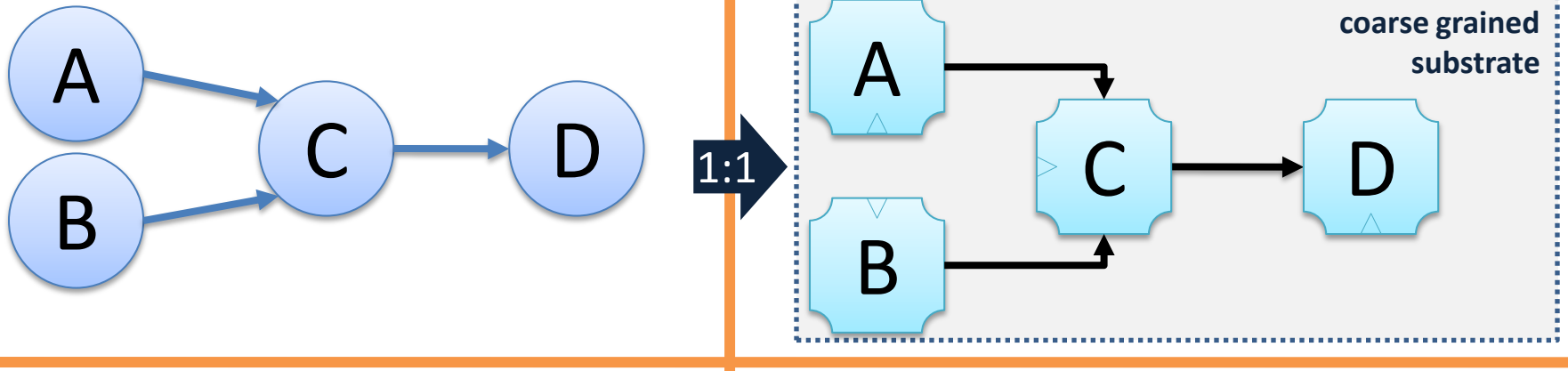
MP3, Camera, Video, GPS...

MARKET DEMAND

convenient form factor, affordable price, fashion

MDC tool Summary

Approach



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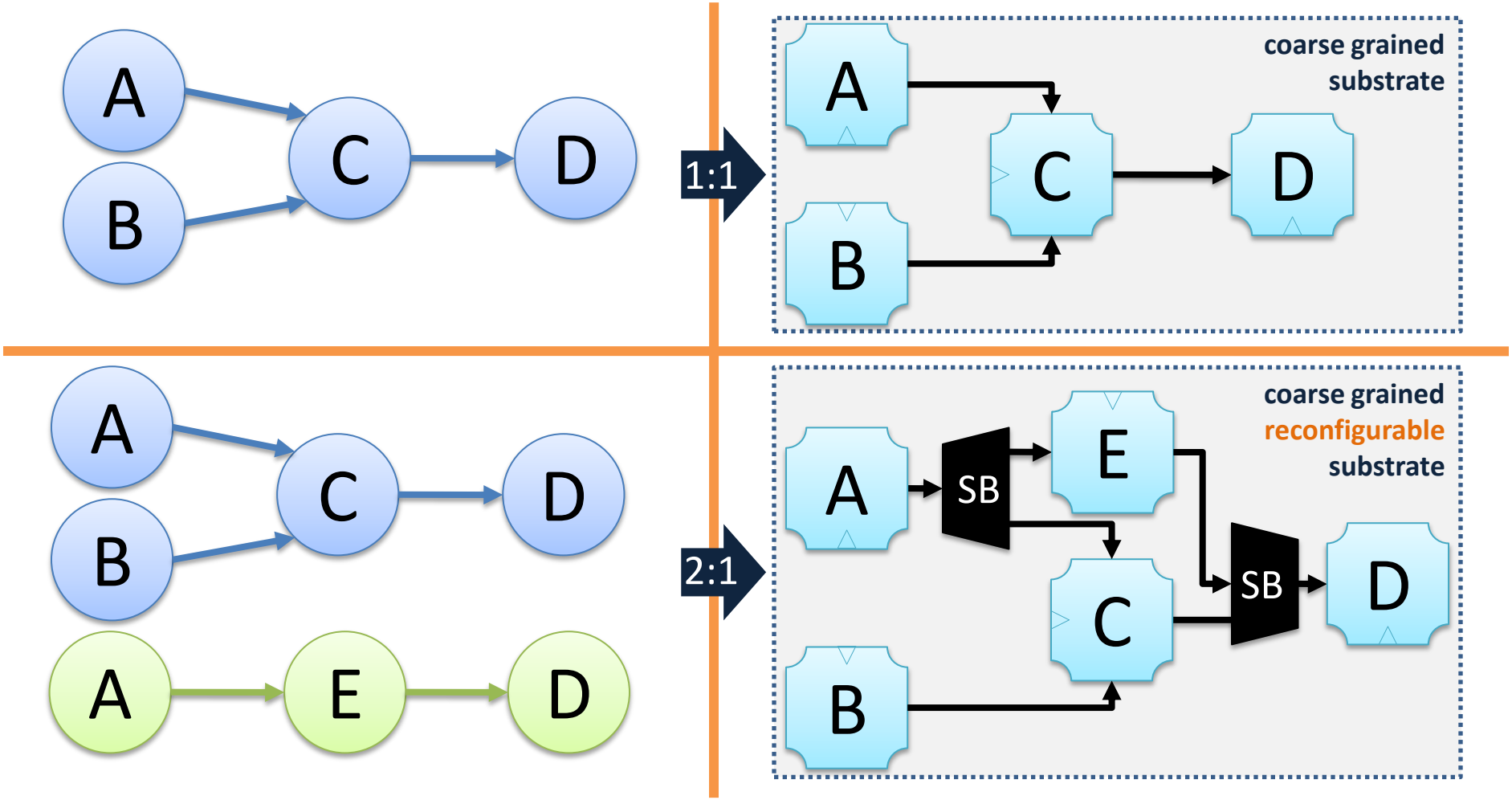
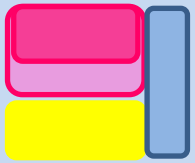
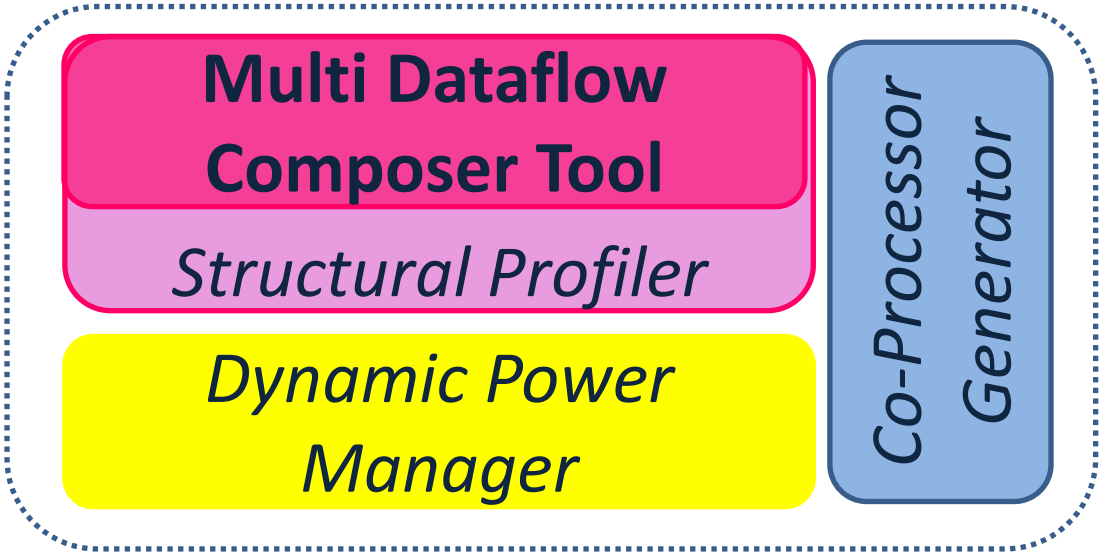


MDC tool Summary

Current Functionalities





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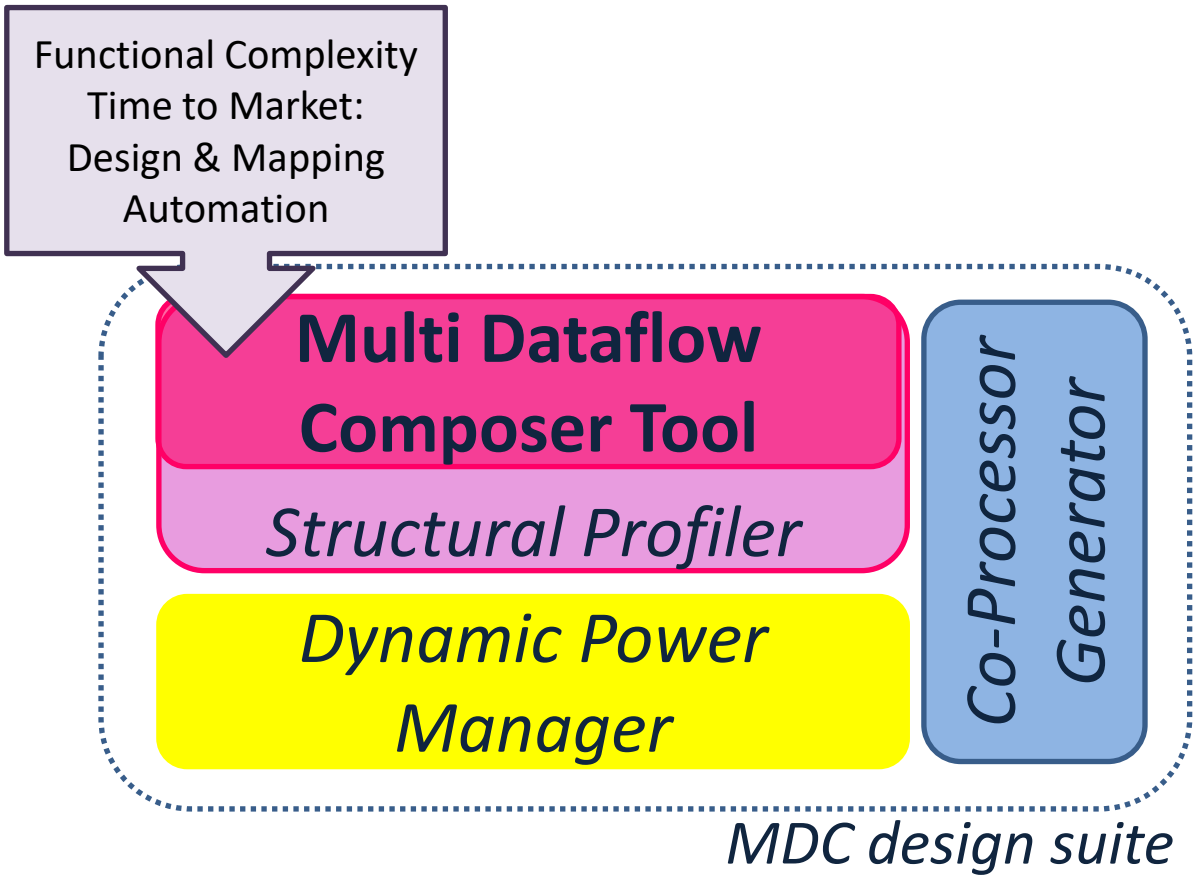

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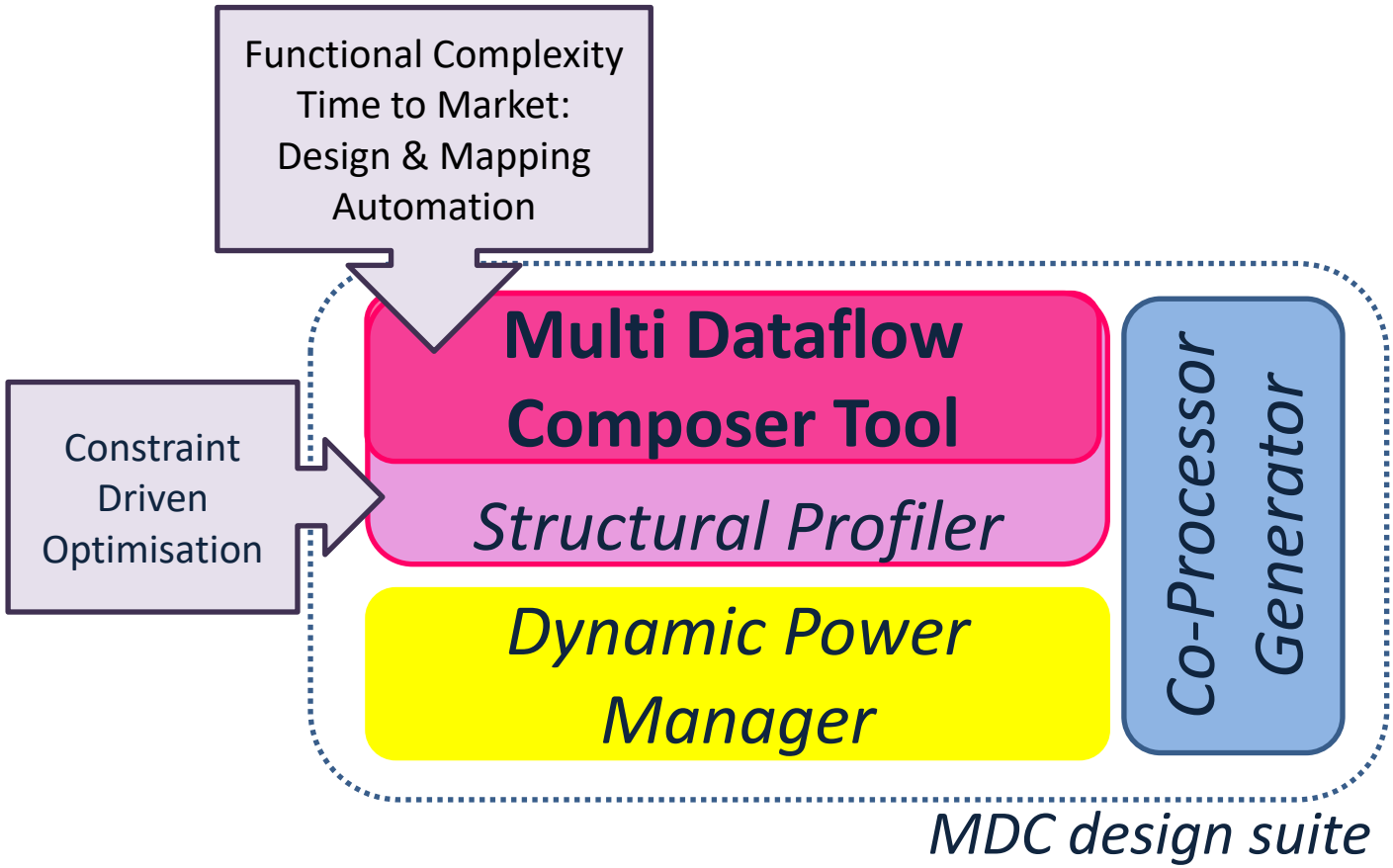

http://sites.unica.it/rpct/

MDC tool Summary

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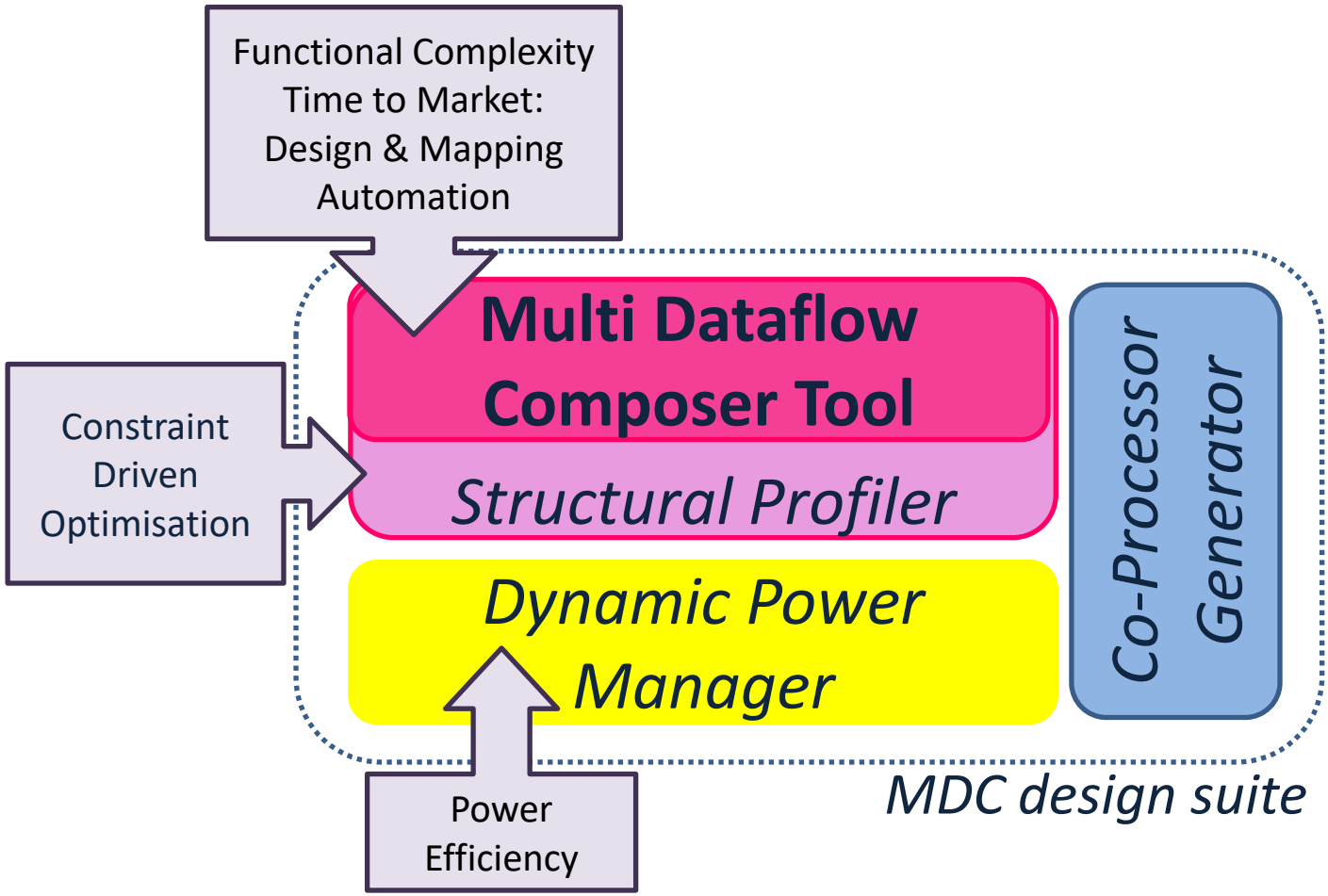

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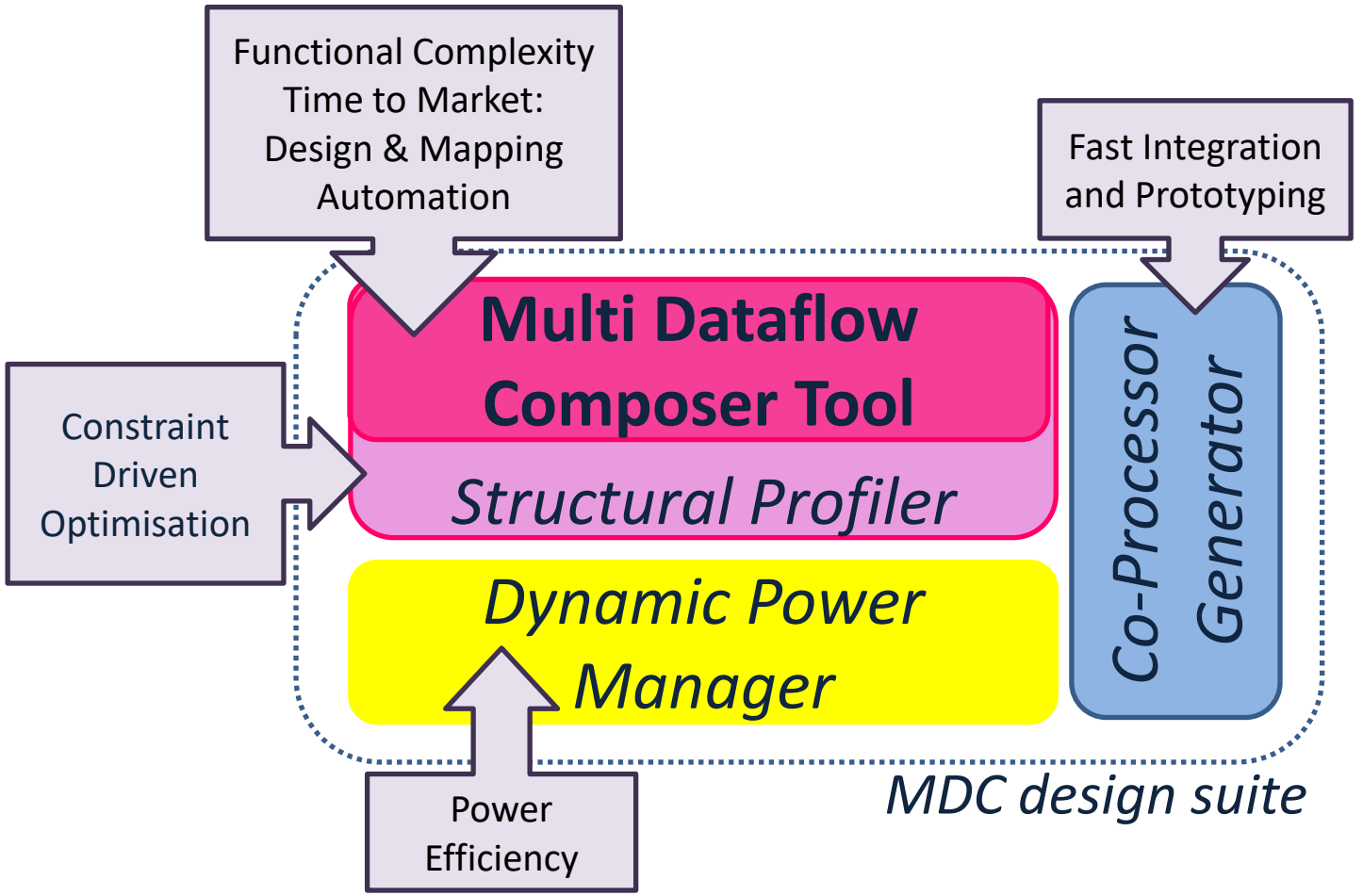

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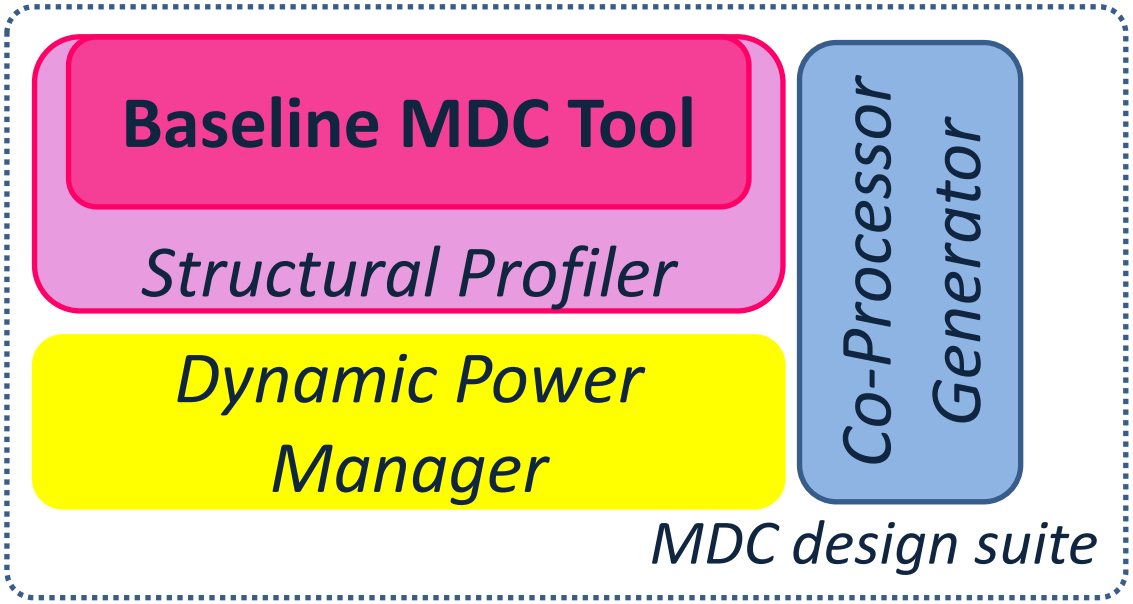

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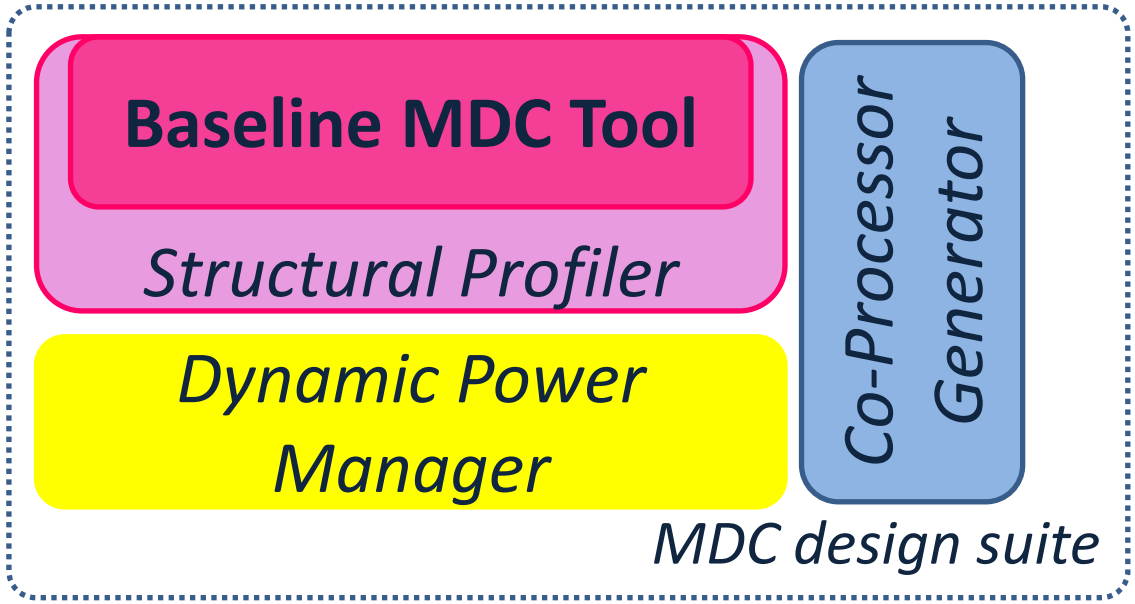

HW/SW Partitioning

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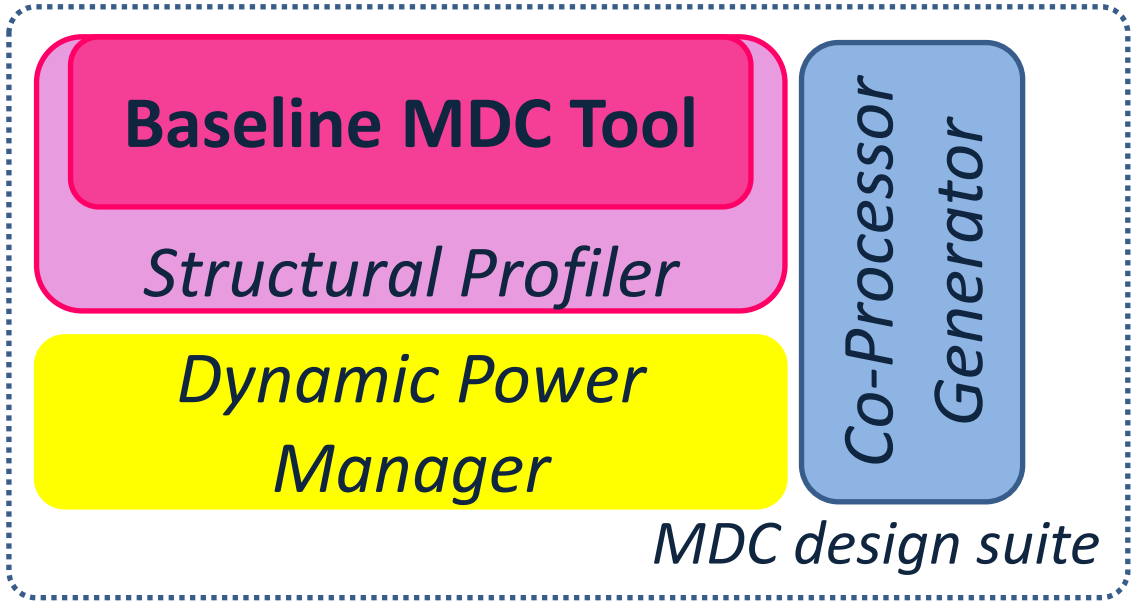

HW/SW Partitioning

Enhancing HLS

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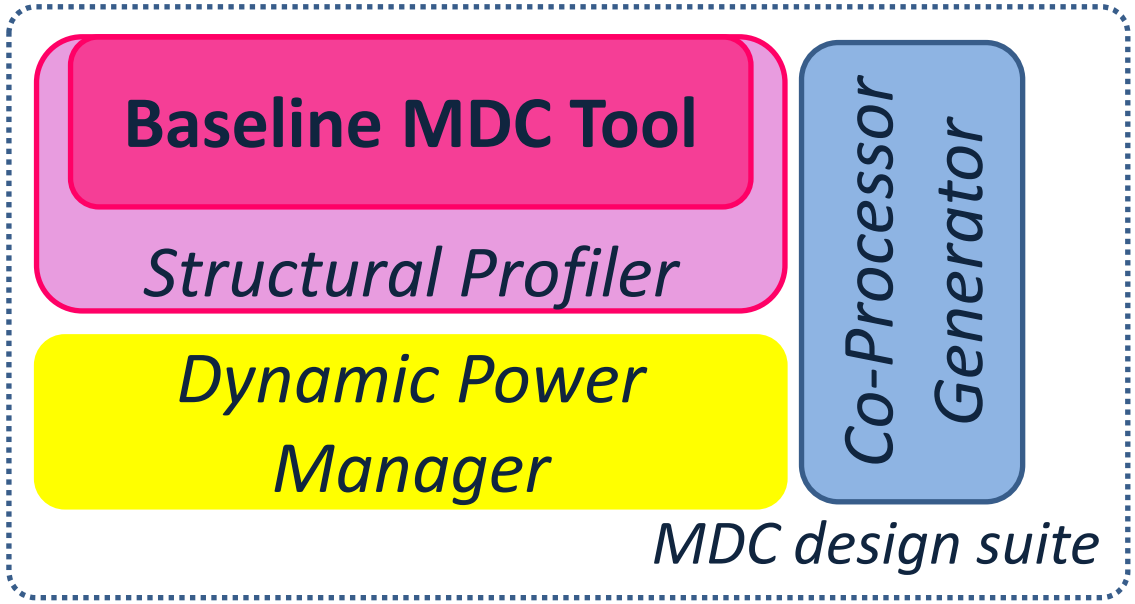

- HW/SW Partitioning
- Enhancing HLS
- Runtime Monitoring

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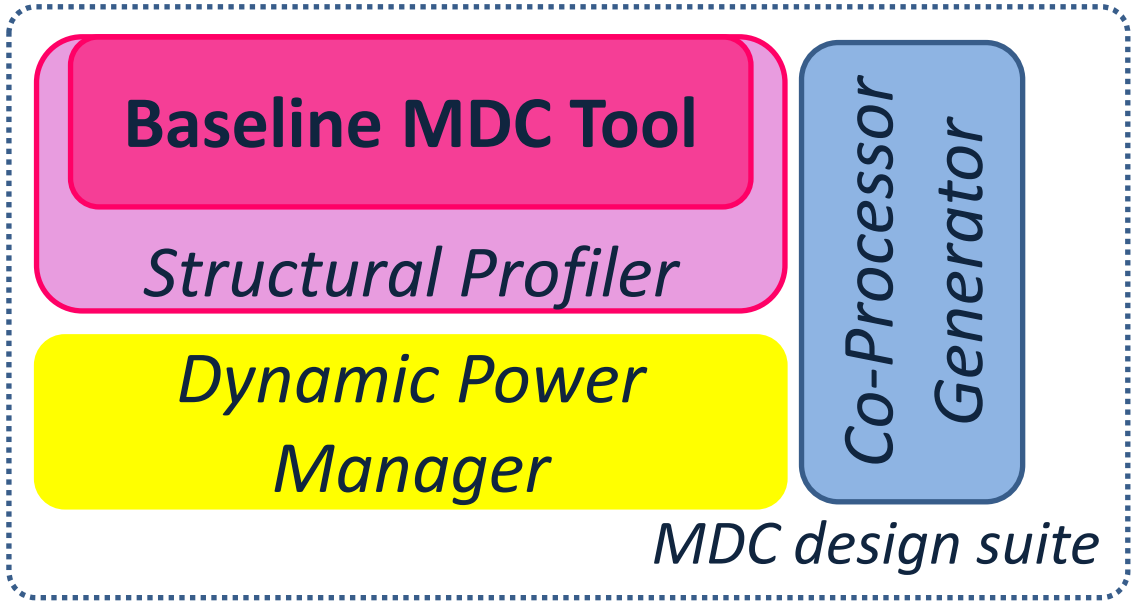

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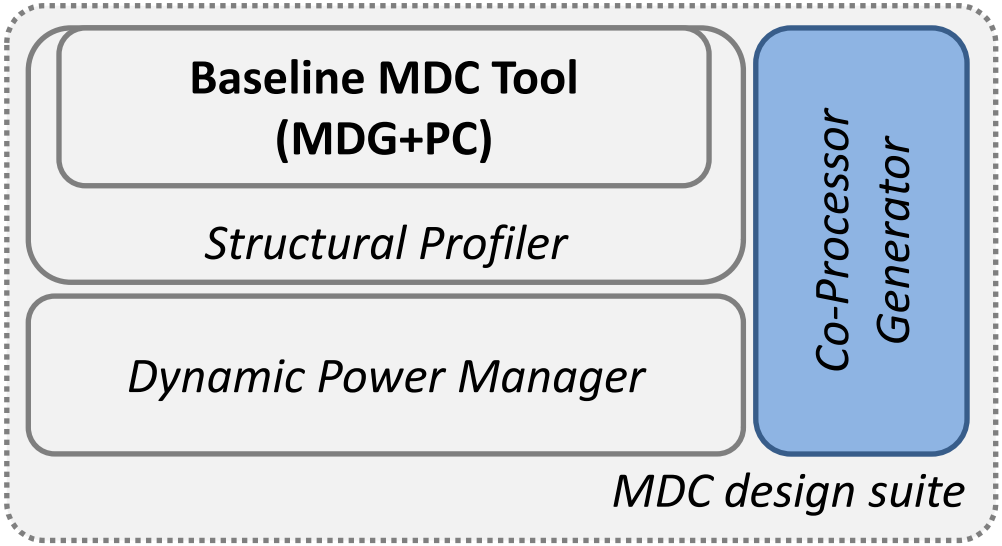
Hardware-Software Partitioning

Co-Processing Support



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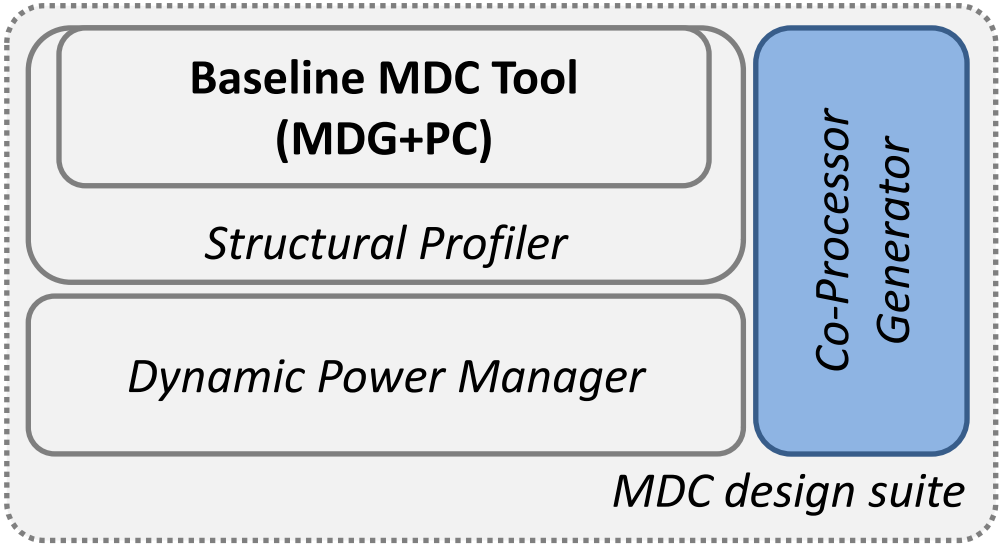
Hardware-Software Partitioning

Co-Processing Support



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Hardware-Software Partitioning

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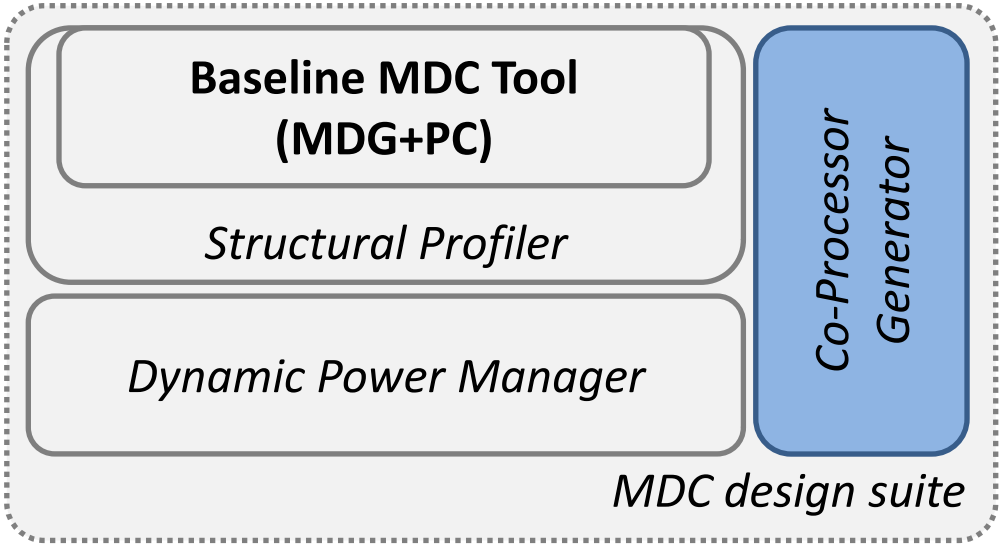

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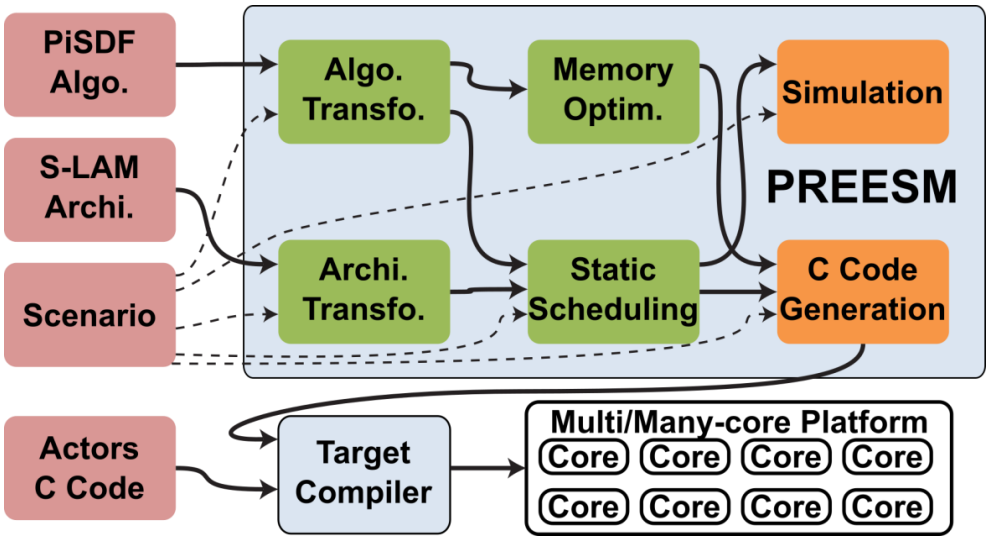
- MDC assembles **ready-to-use platform-dependent IPs**

- Designer can choose to opt for **memory-mapped** or **stream-based** coupling.

Hardware-Software Partitioning

Automated Characterization



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It provides mapping of actors to multiple processing cores, optimizing execution latency and balancing loads.

Hardware-Software Partitioning

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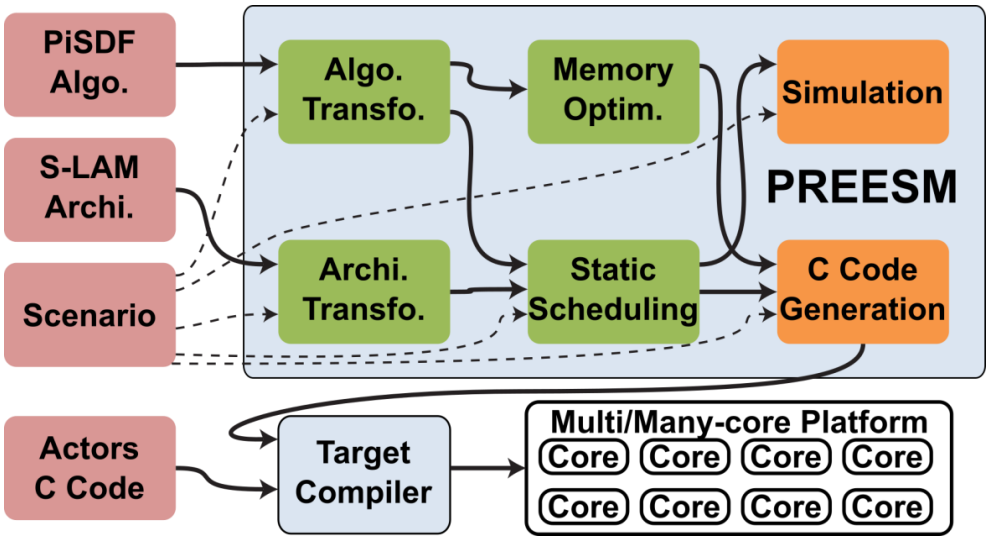

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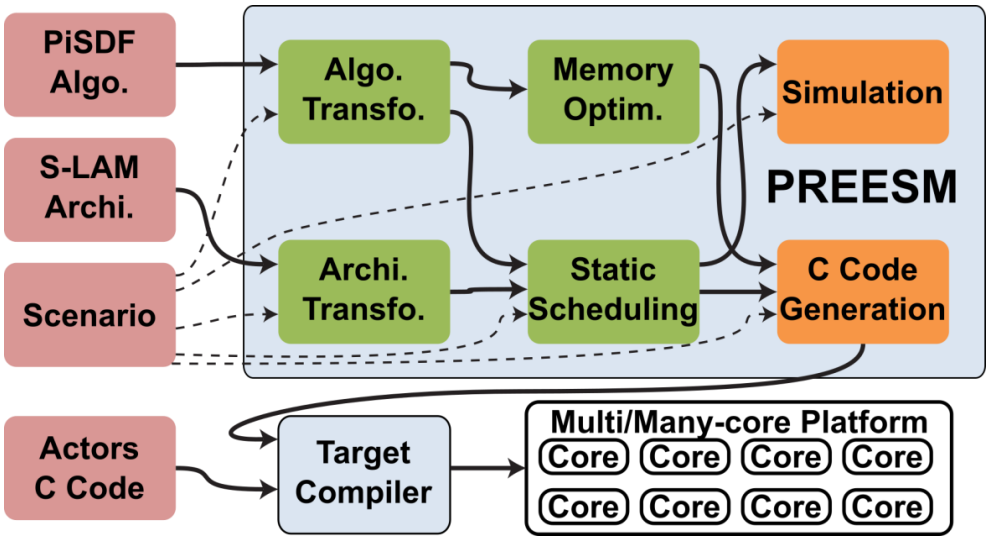

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- **Connect PREESM and MDC** to delegate specific computations (an actor, a network of actors or a set of networks) to the most suitable co-processing units

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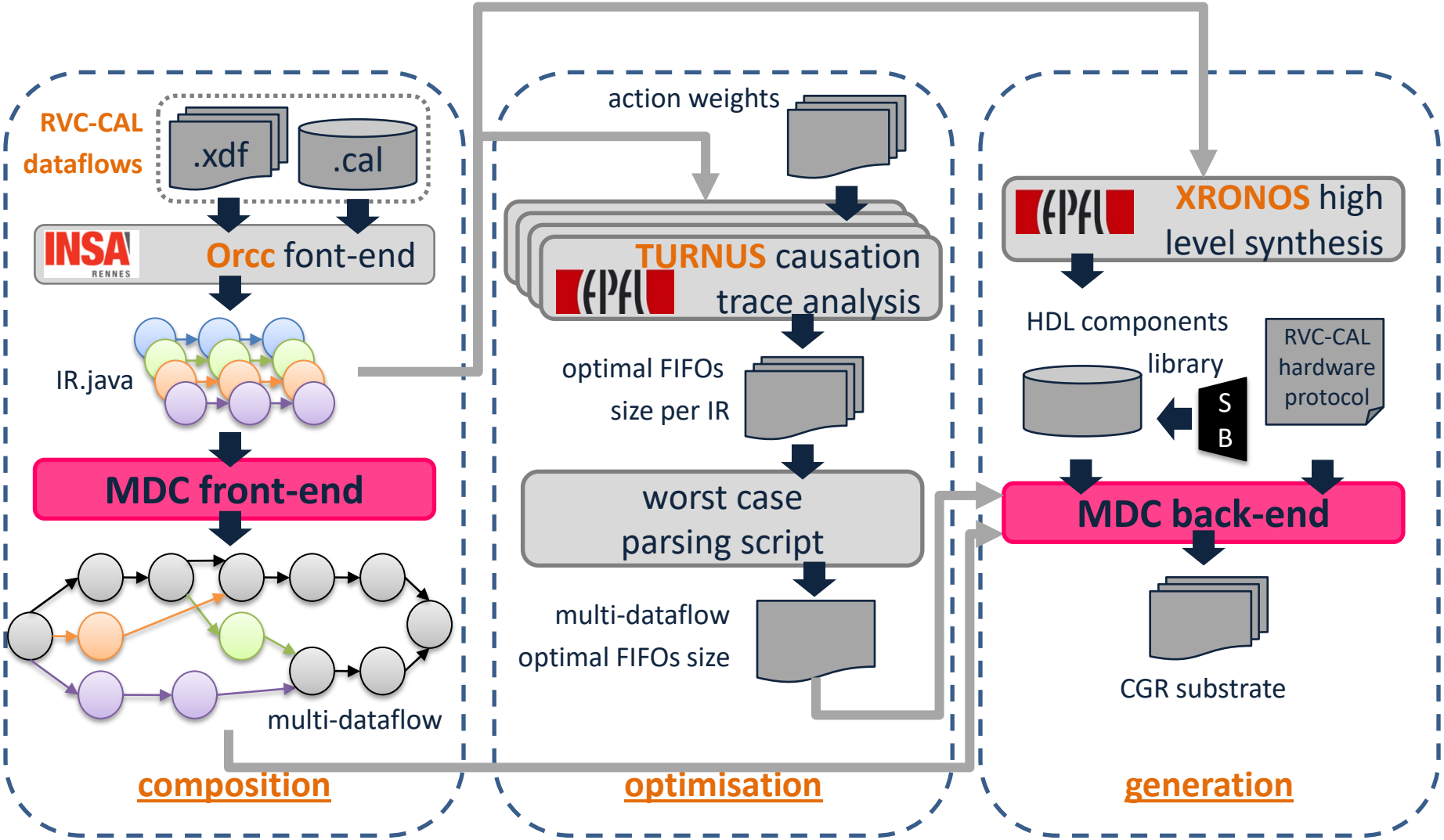
Enhancing MDC High-Level Synthesis Support

Previous Fully Automated Flow



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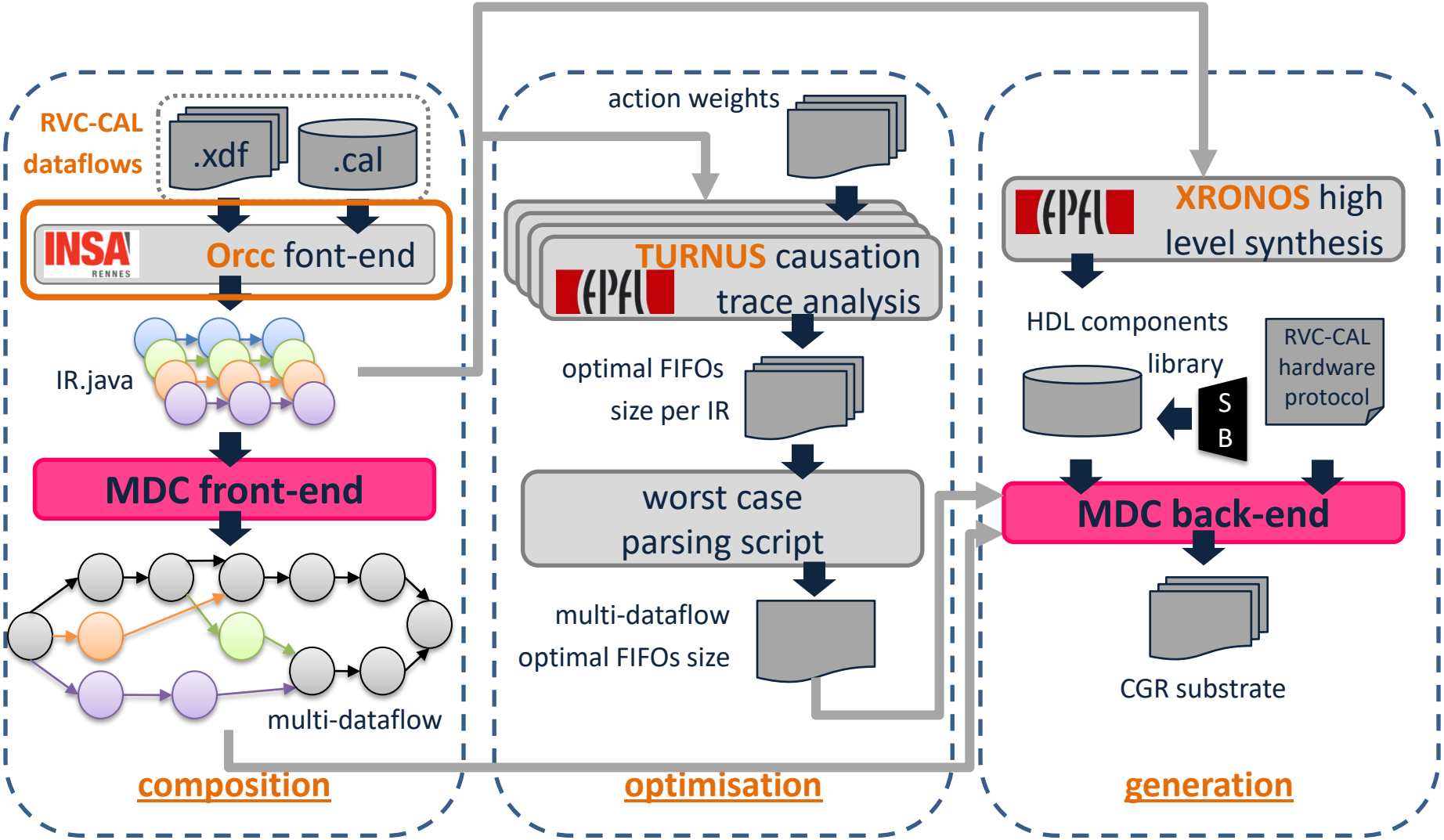

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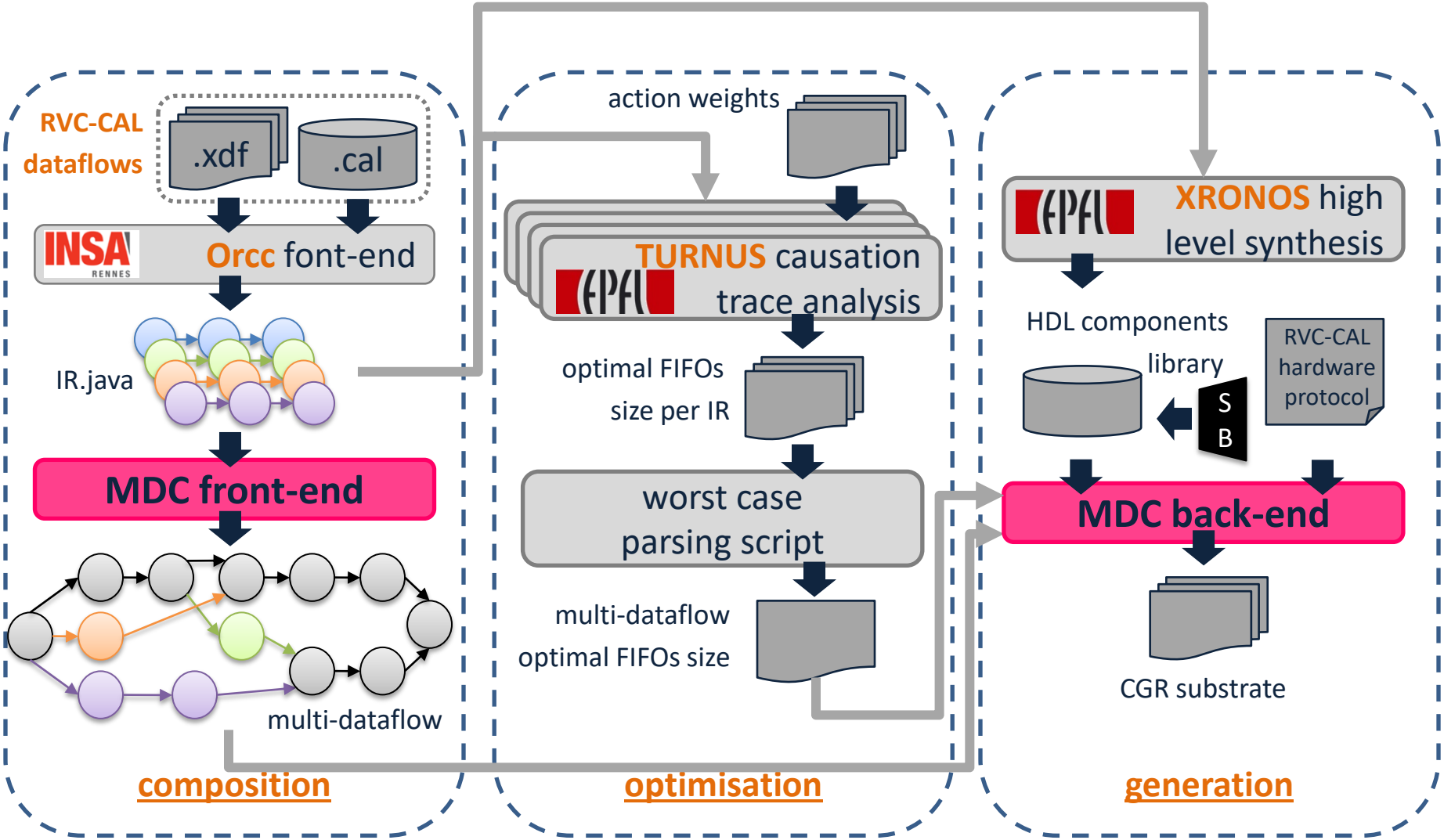

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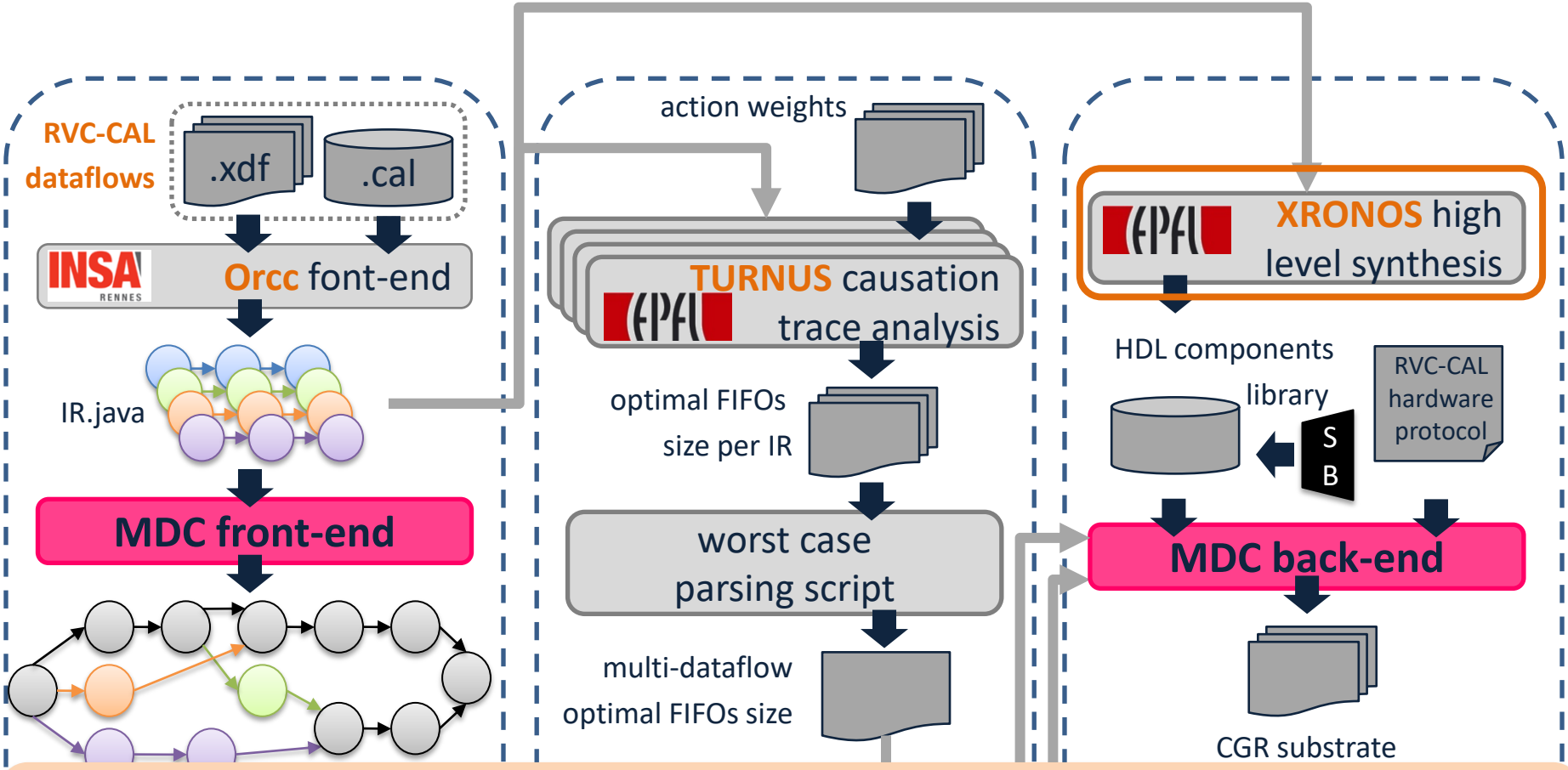

- High-Level Synthesis supports **only FPGAs from one specific FPGA vendor (Xilinx)**

Enhancing MDC High-Level Synthesis Support

CAPH

- CAPH is a domain-specific language for describing and implementing stream-processing applications.

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CAPH SOURCE CODE

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-- Global values declarations (libraries, variables, constants, functions, types)
#include "dc.cph"

-- Actor declarations
actor inv
in ( i : unsigned<8> dc )
out ( o : unsigned<8> dc )
rules
| i:'< -> o:'<
| i:'> -> o:'>
| i:' x -> o:'255-x ;

-- I/O declarations
stream inp: unsigned<8> dc from "sample.txt";
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-- Network declarations
net outp = inv inp;
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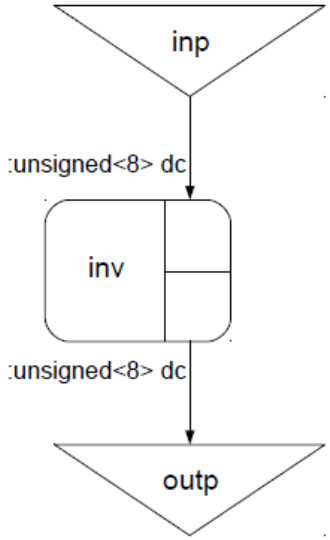
CAPH GRAPH



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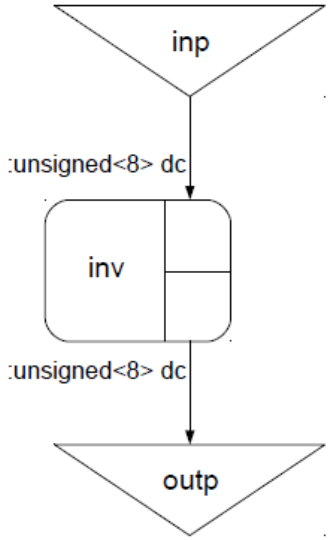

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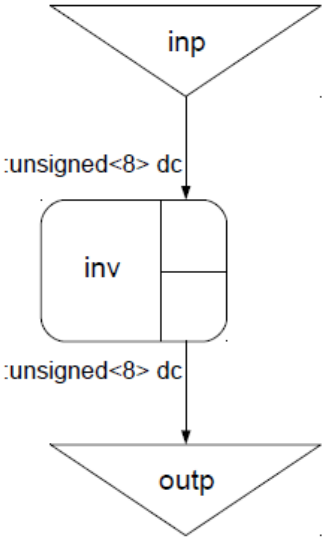

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- It is capable of **generating VHDL code**

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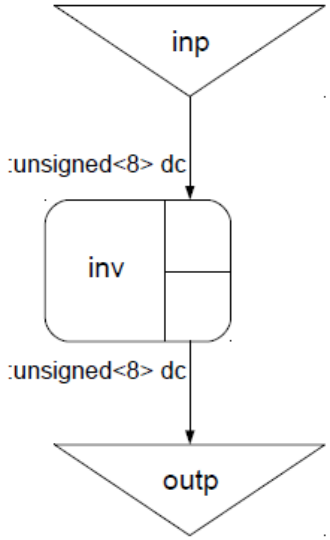

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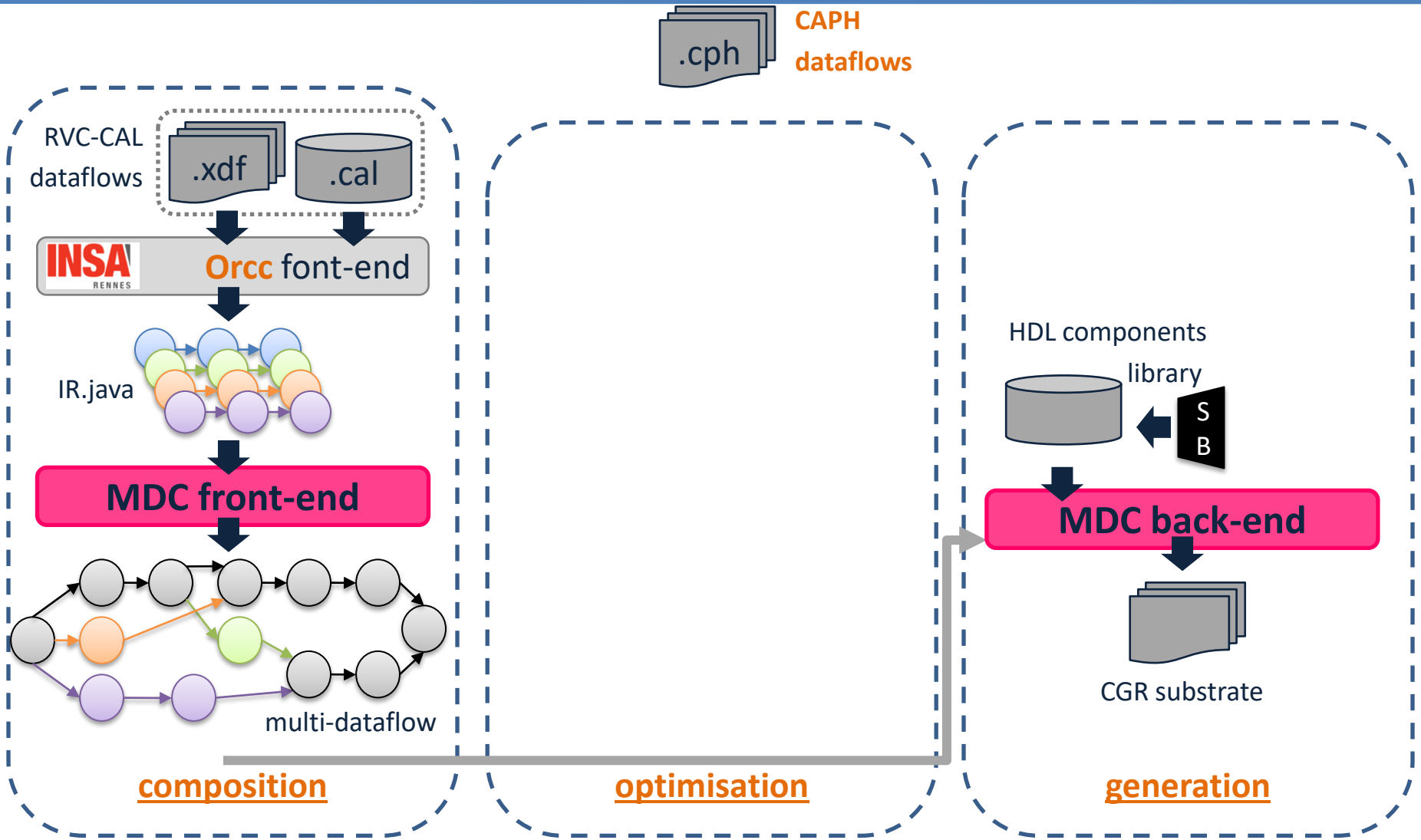
- It is capable of **generating VHDL code**
- It is **platform agnostic**

Enhancing MDC High-Level Synthesis Support

Fully Automated Flow



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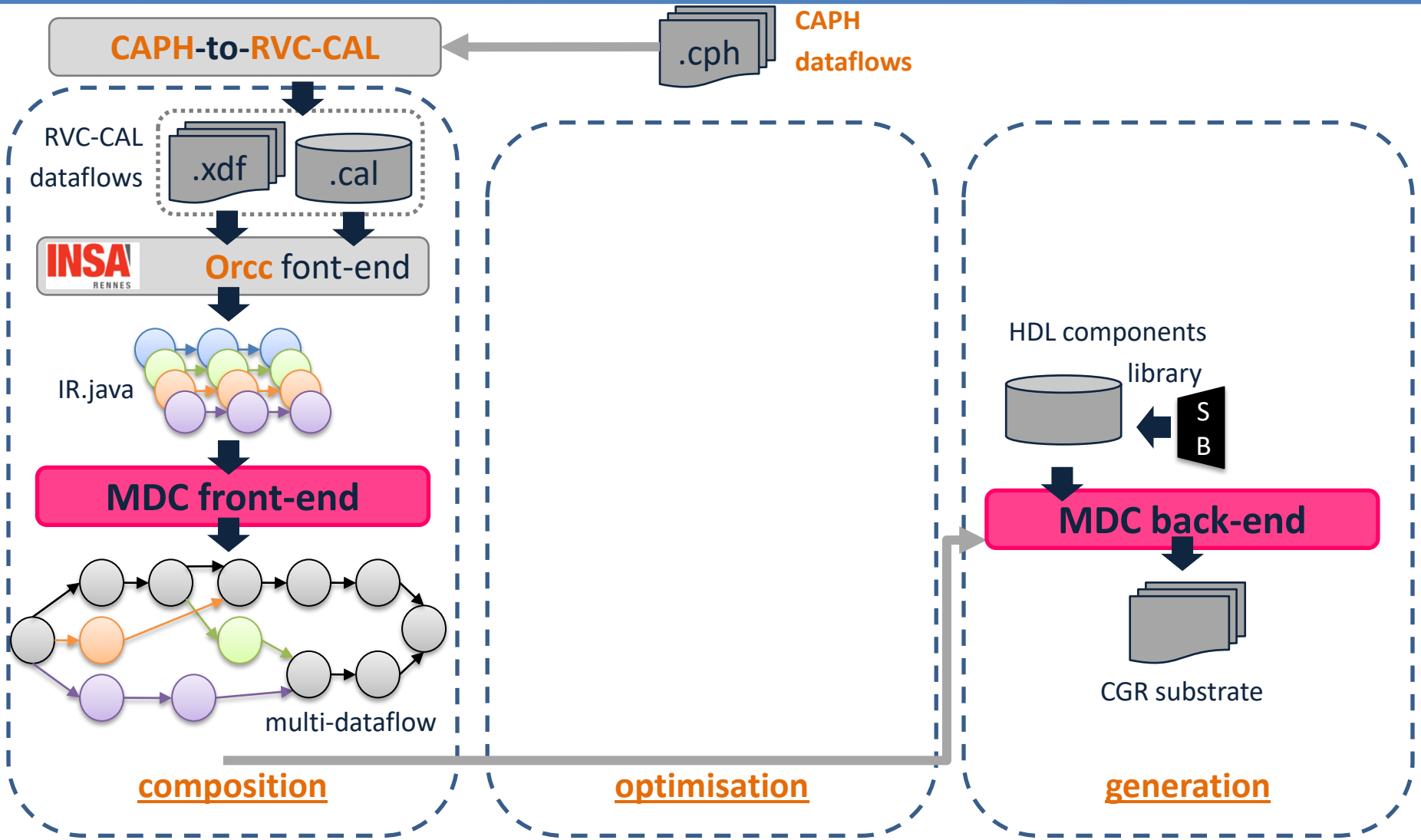

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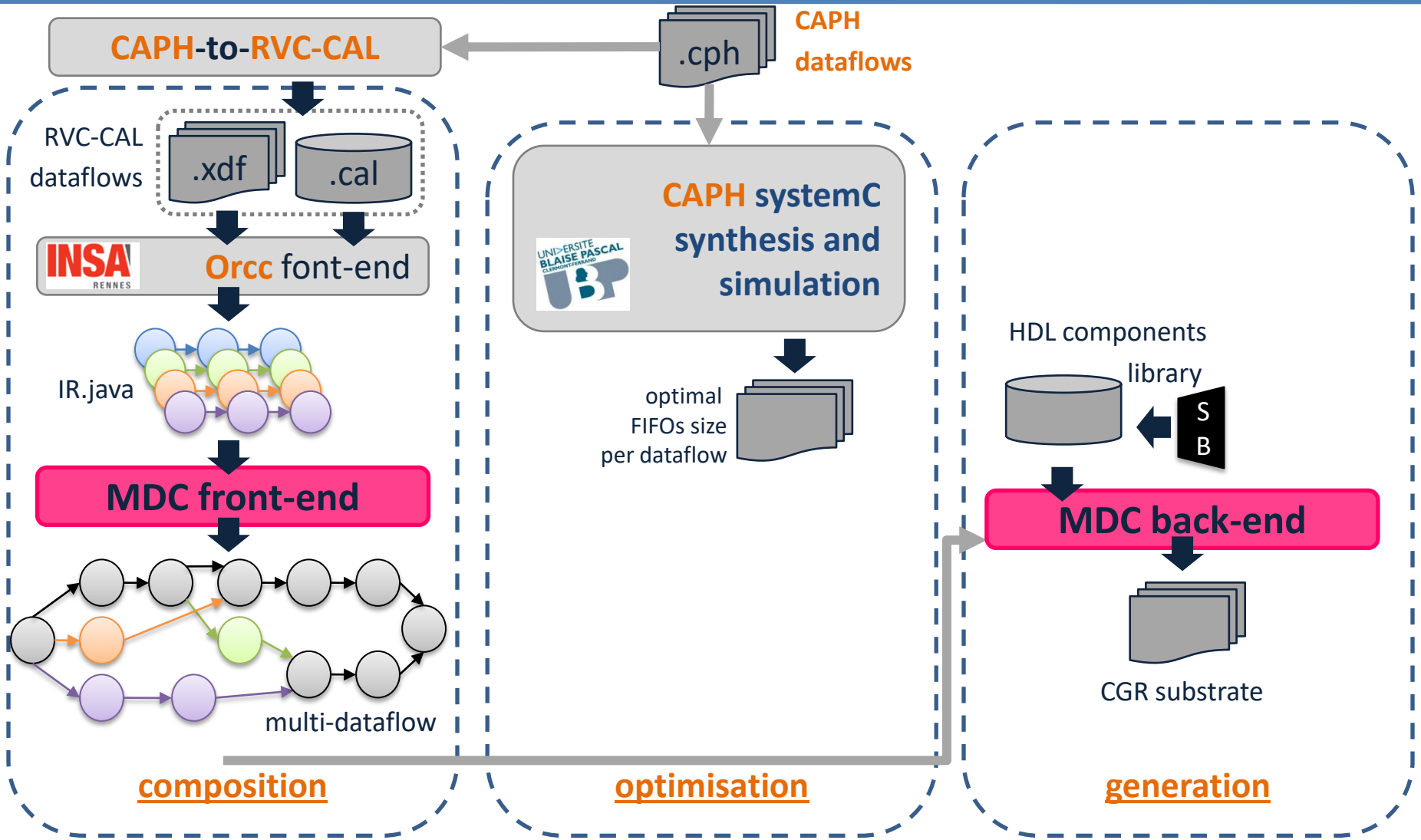

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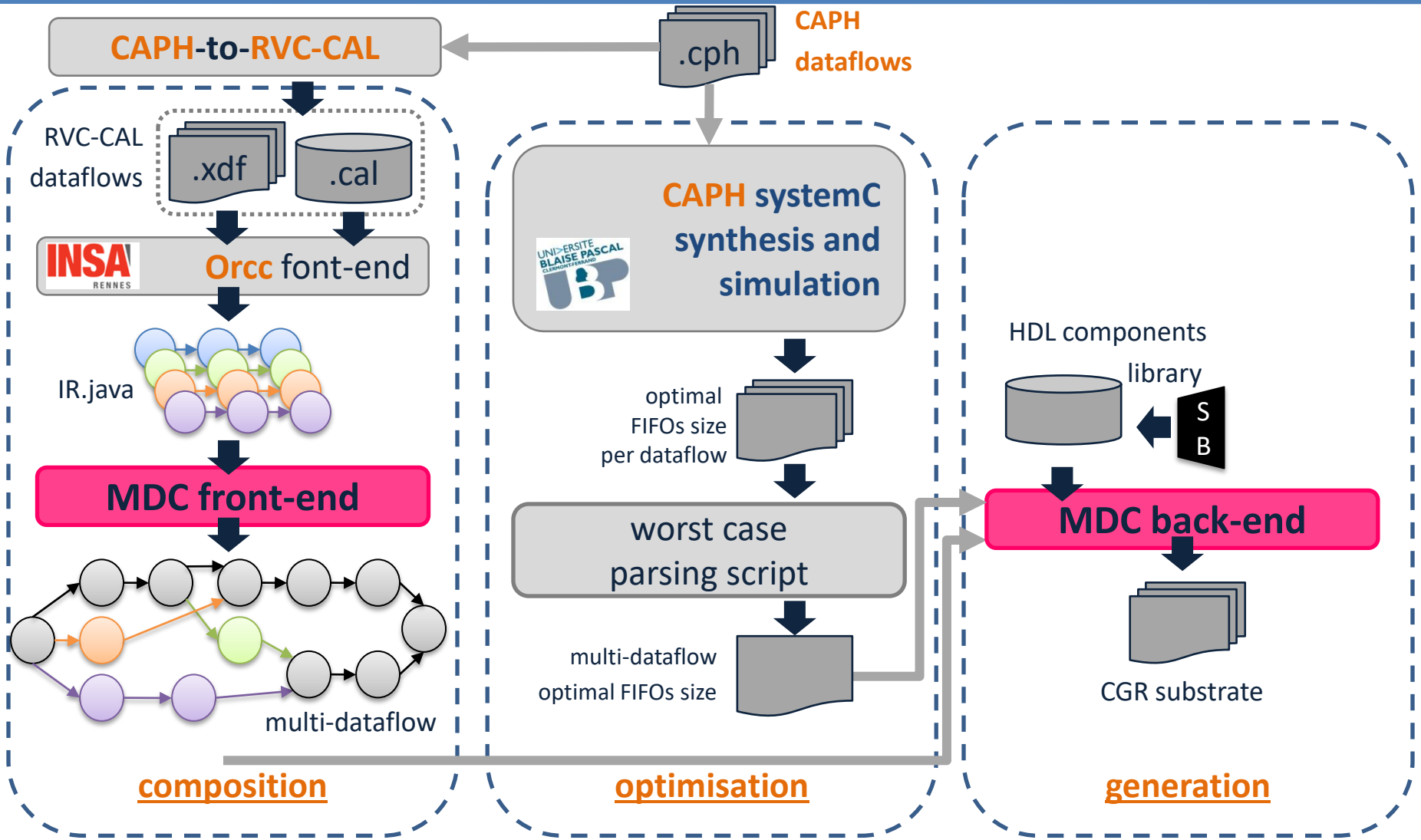

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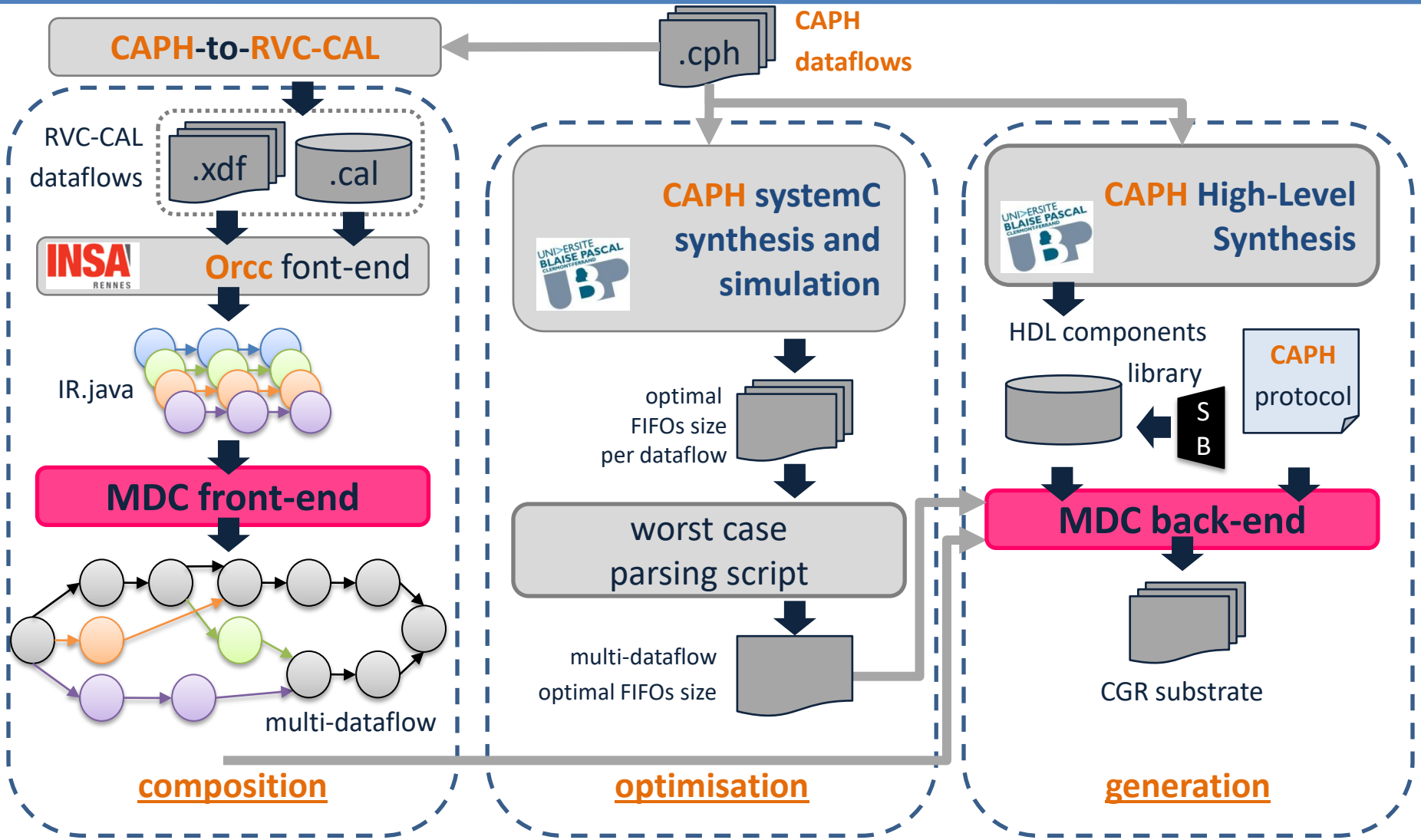

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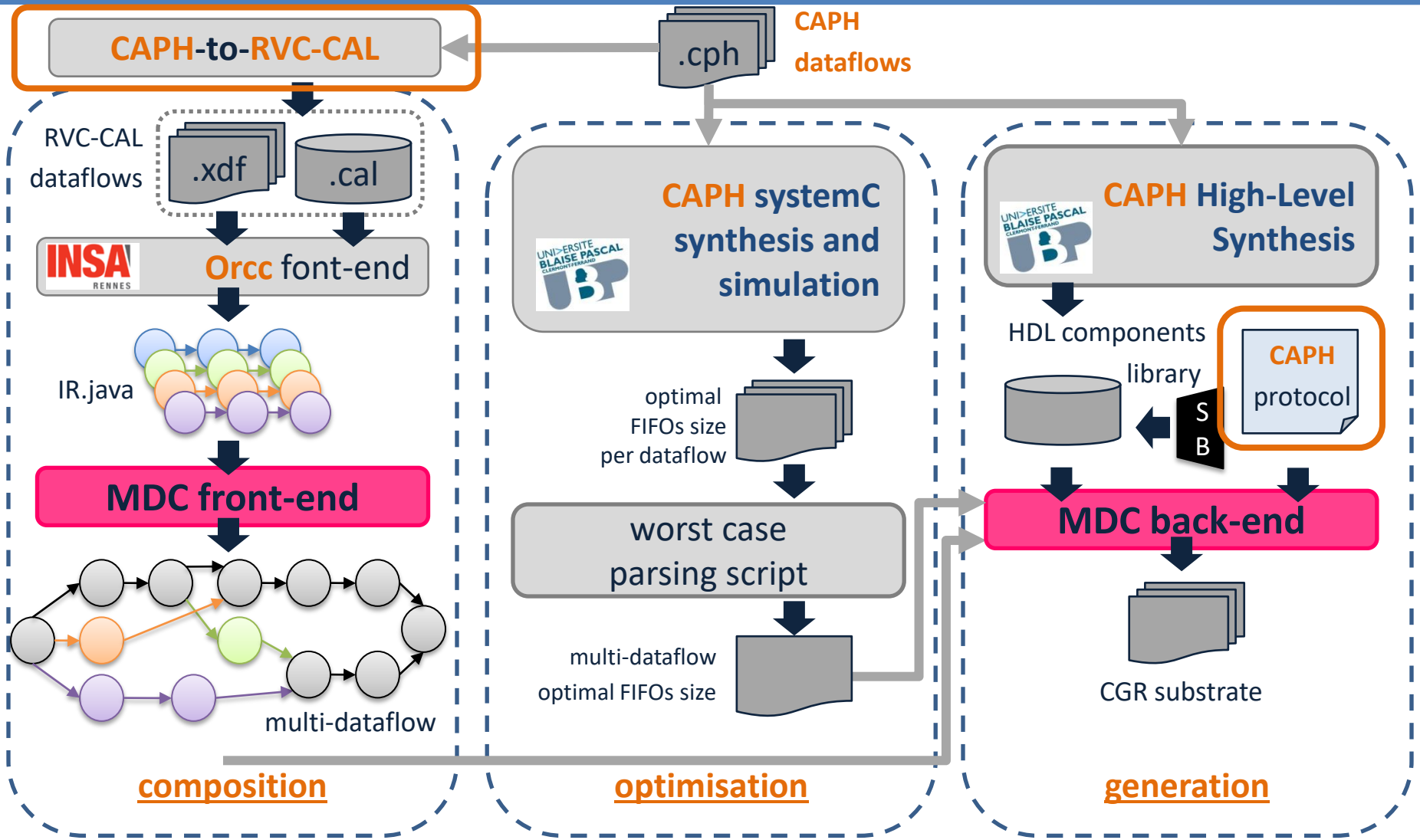

Enhancing MDC High-Level Synthesis Support

Protocol Generalization

```
<protocol>
  <sys_signals>
    <signal id="0" net_port="clock"  is_clock=""…></signal>
    …
  </sys_signals>
  <actor>
    <sys_signals>
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      …
    </sys_signals>
    <comm_signals>
      <signal id="0" port="din" channel="data"…></signal>
      <signal id="1" port="dout" channel="data"…></signal>
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 <predecessor>
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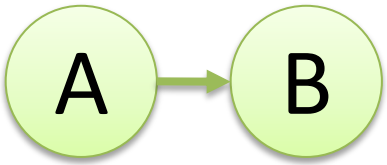

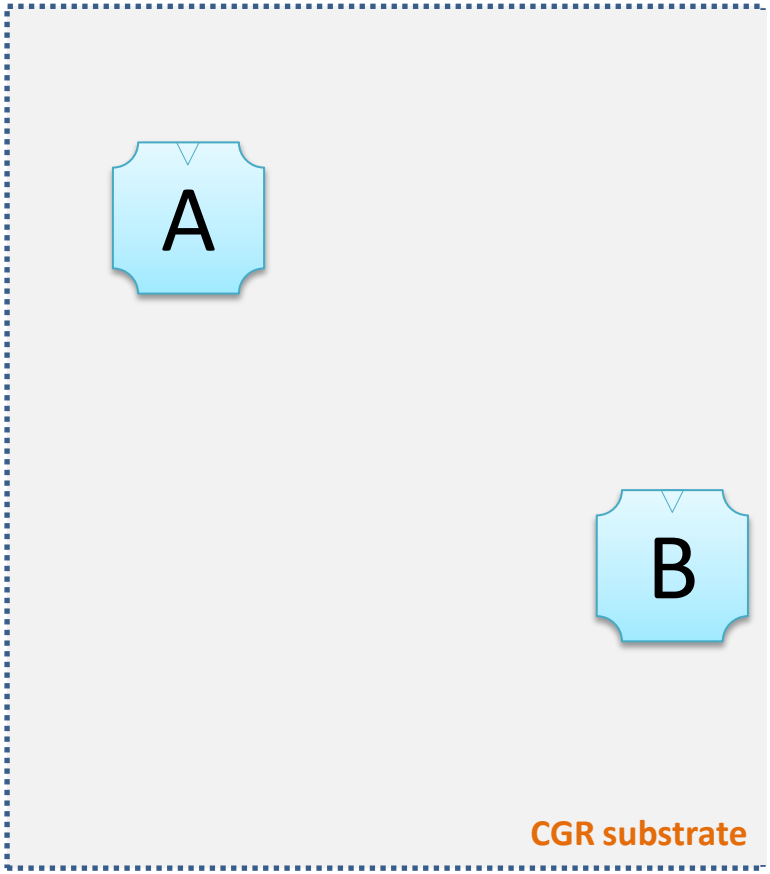

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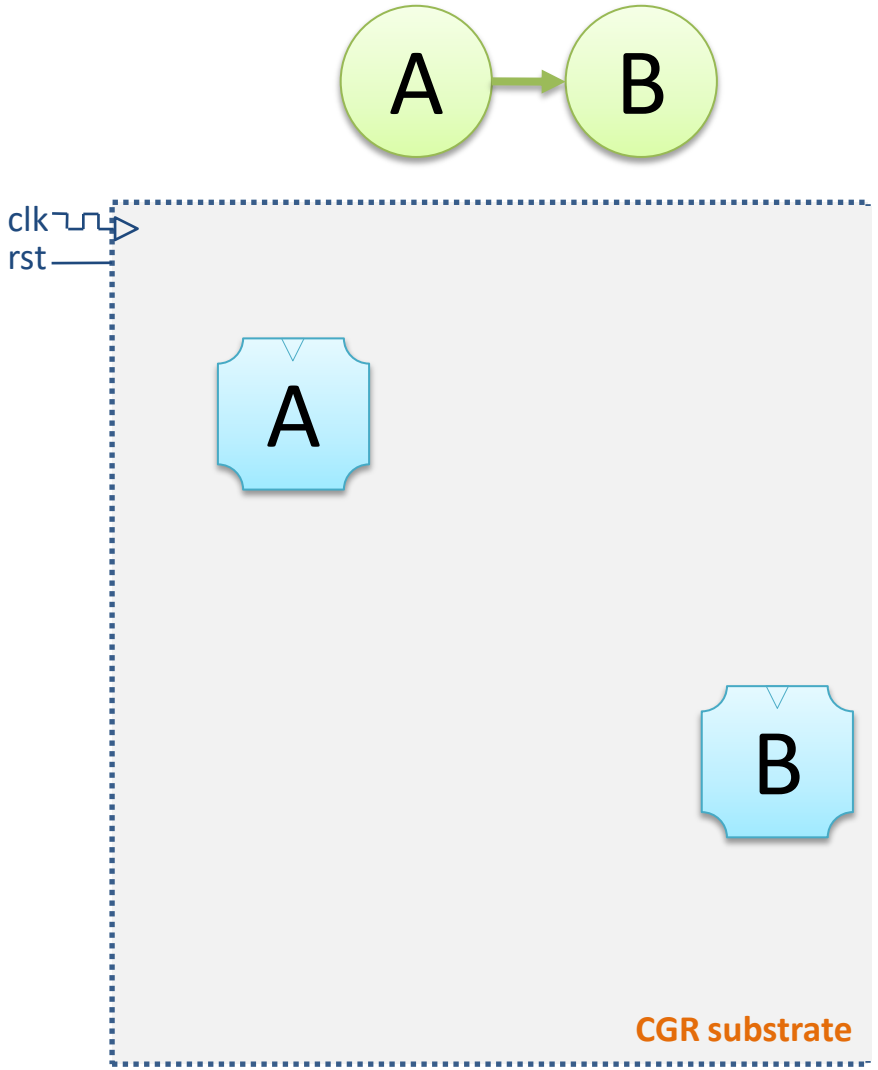

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    <sys_signals>…</sys_signals>
    <comm_signals>…<comm_signals>
  </predecessor>
  <successor>
    <sys_signals>…</sys_signals>
    <comm_signals>…<comm_signals>
  </successor>
</protocol>
```

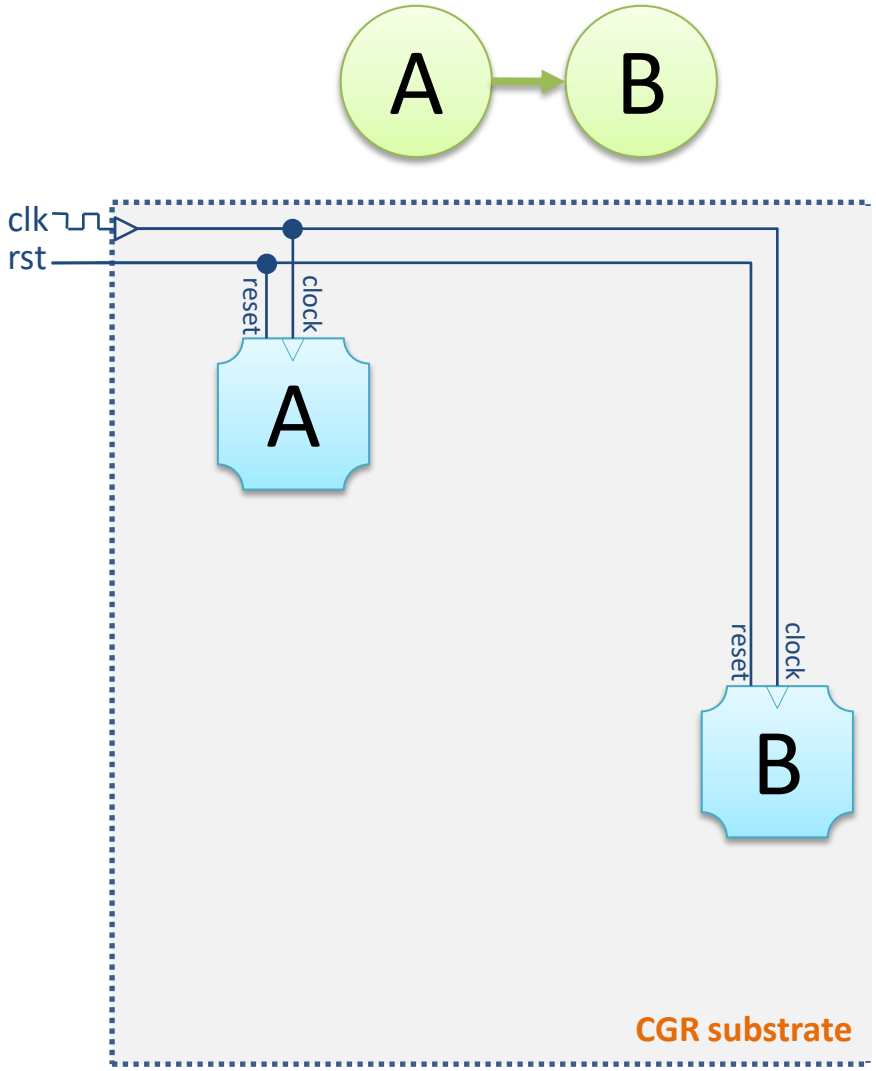

Enhancing MDC High-Level Synthesis Support

Protocol Generalization

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<protocol>
  <sys_signals>
    <signal id="0" net_port="clock"  is_clock=""…></signal>
    …
  </sys_signals>
  <actor>
    <sys_signals>
      <signal id="0" port="clk" net_port="clock" …></signal>
      …
    </sys_signals>
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      <signal id="0" port="din" channel="data"…></signal>
      <signal id="1" port="dout" channel="data"…></signal>
      <signal id="2" port="wr" channel="en"…></signal>
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    <comm_signals>
  </actor>
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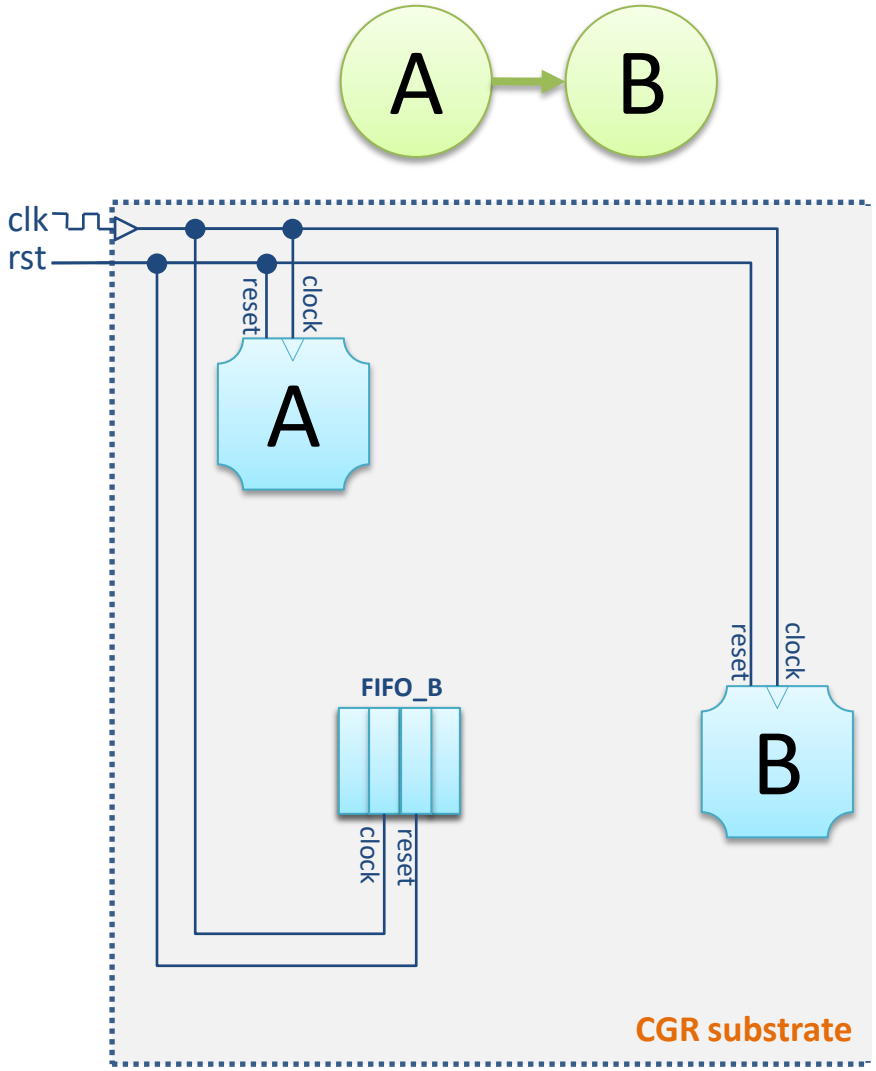

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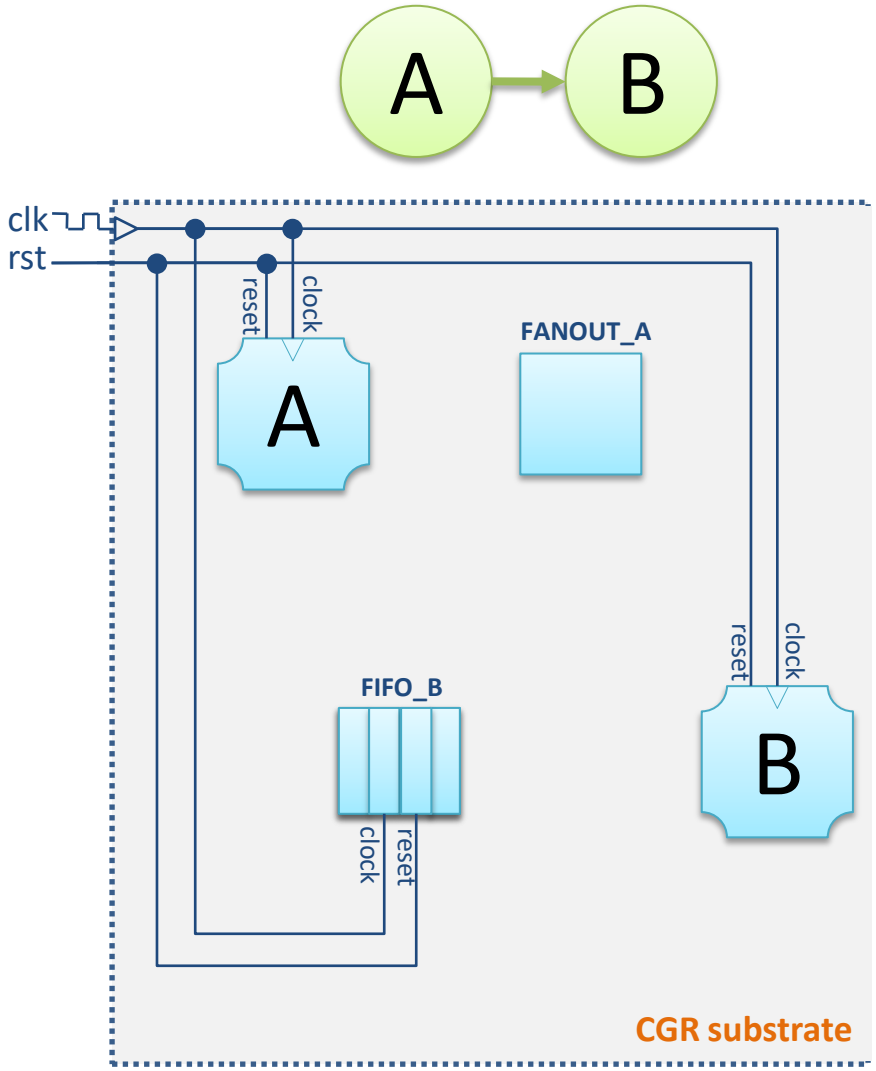

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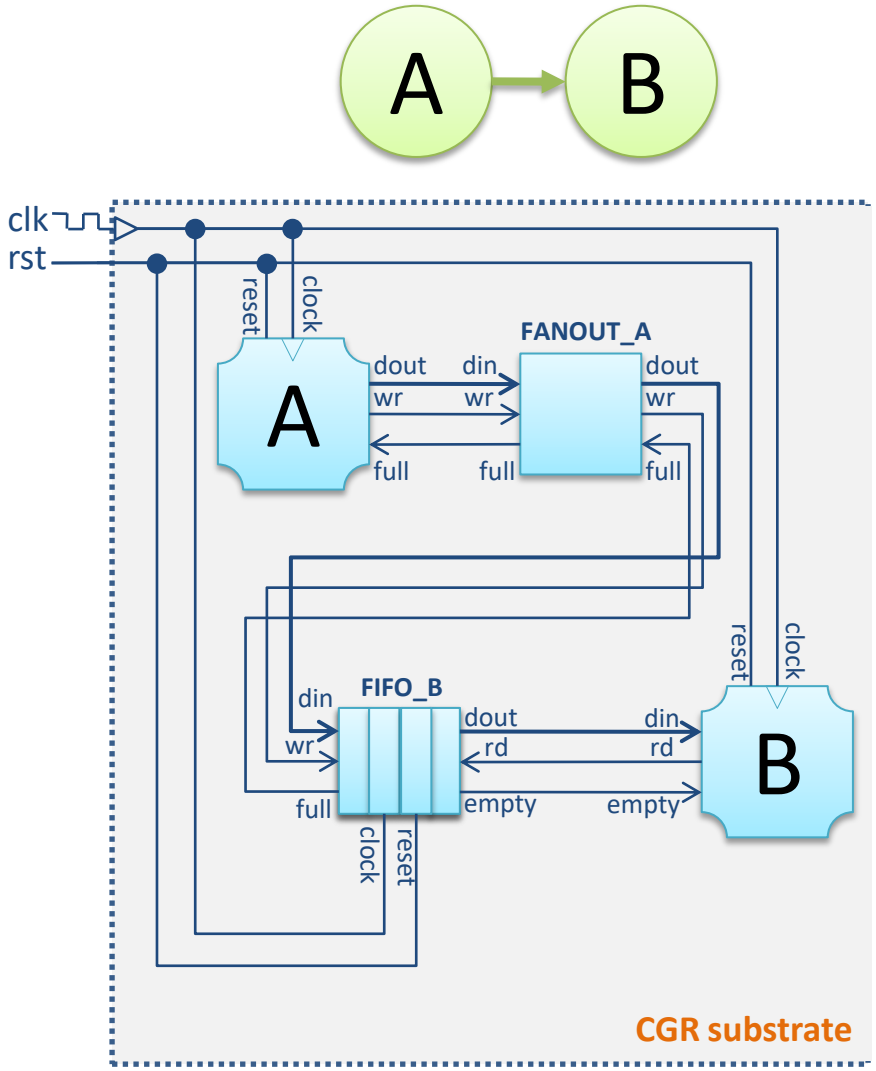


Enhancing MDC High-Level Synthesis Support

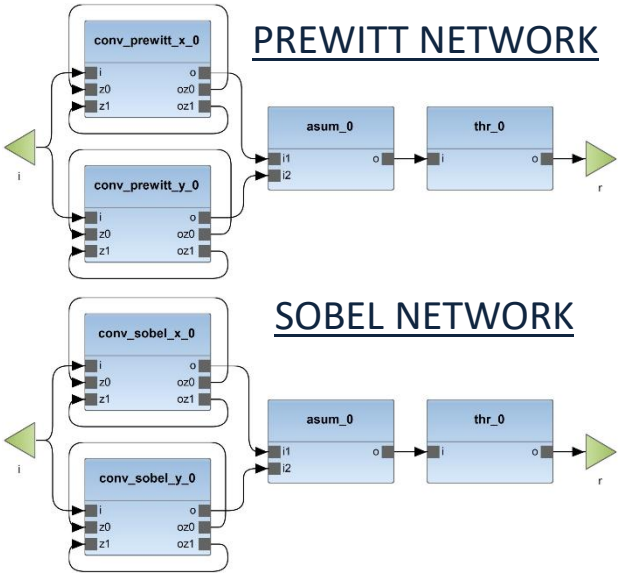
Prewitt/Sobel Multi-Flow Network

Enhancing MDC High-Level Synthesis Support

Prewitt/Sobel Multi-Flow Network

INPUT NETWORKS

(provided by CAPH)



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Prewitt/Sobel Multi-Flow Network

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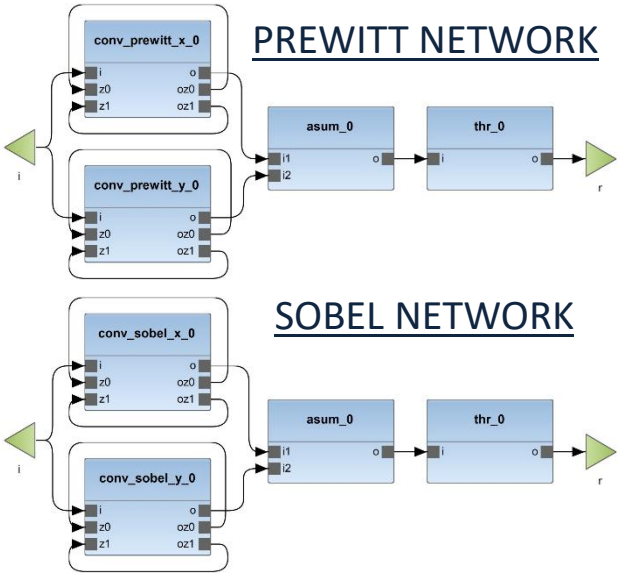

OUTPUT NETWORK
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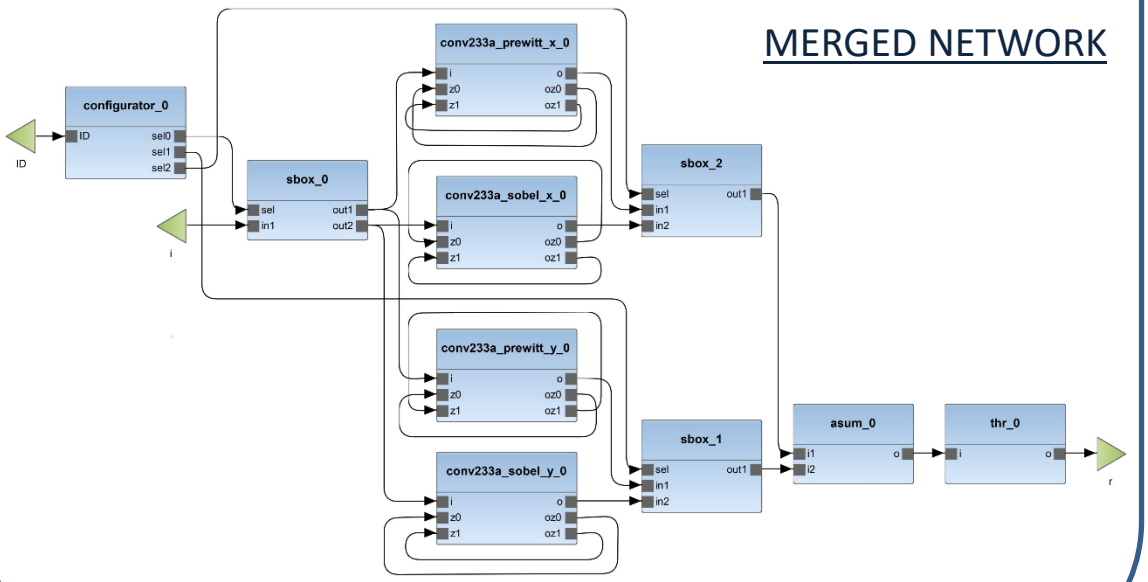

Enhancing MDC High-Level Synthesis Support

Preliminary Results

Enhancing MDC High-Level Synthesis Support

Preliminary Results

FPGA - Altera (5SGSMD5) and Xilinx (XC7VX485T)

RESOURCES	MDC+CAPH		MDC+XRONOS		XRONOS vs CAPH	
	Altera	Xilinx	Altera	Xilinx	Altera	Xilinx
REG	1484	780	-	632	-	-18,97%
LOGIC	1047	2347	-	1533	-	-34,68%
RAM	15	0	-	6.5	-	+100%
DSP	36	36	-	0	-	-100%
MAX FREQ [MHz]	105,80	93,69	-	142,86	-	+58,50%
EXEC TIME [cck]	15340	15340	-	15348	-	+0,05%

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ASIC - TSMC 45 nm CMOS technology

	Prewitt/Sobel	Multi-Flow
AREA [kGE]	269,82	466,90 (+73%)
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COMING SOON:

EXPLORATION ON THE BENEFITS OF DATAFLOW-BASED HLS IN CGR ARCHITECTURES ON THE ROAD

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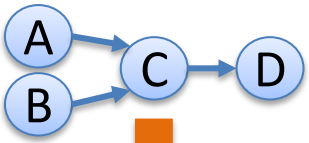
Run-time Monitoring of CGR Accelerators

PAPI for dataflow in software



dataflow application
(RVC-CAL)

C code generation

PROCESSOR
C code
processing

Run-time Monitoring of CGR Accelerators

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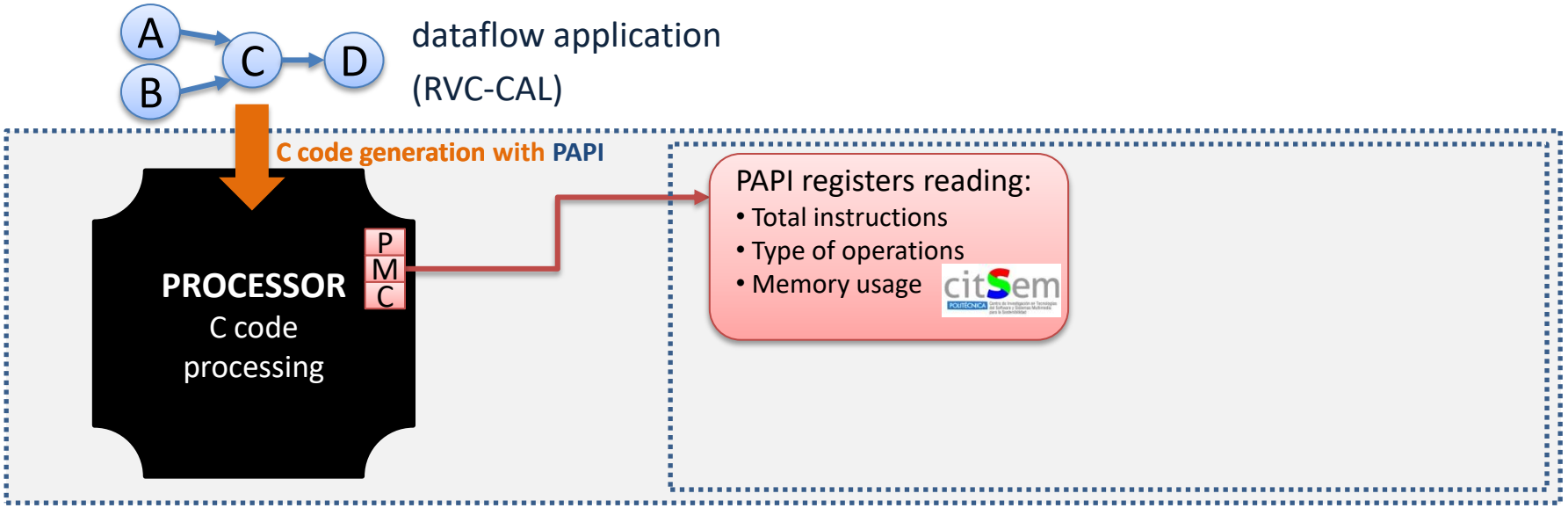

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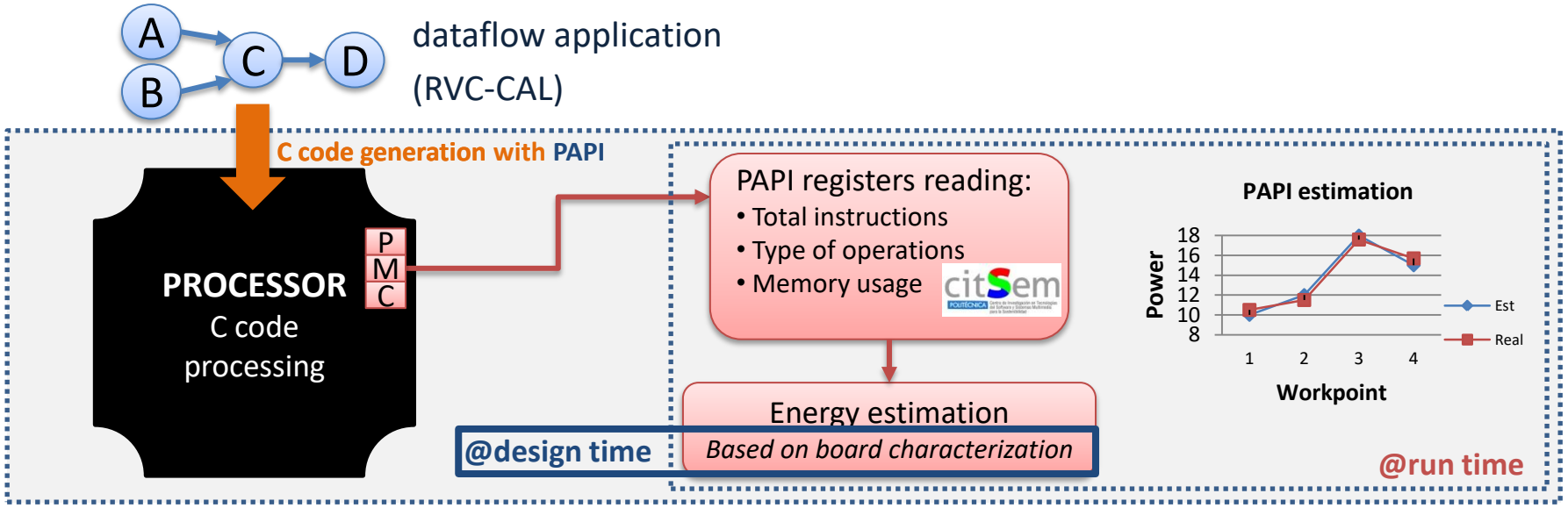

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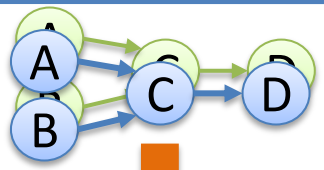

dataflow applications
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C code generation with PAPI

PROCESSOR
C code
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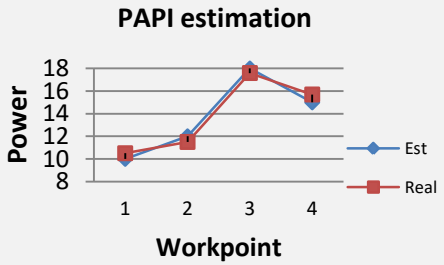
P
M
C

PAPI registers reading:
- Total instructions
- Type of operations
- Memory usage

Energy estimation
Based on board characterization

@design time



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Run-time Monitoring of CGR Accelerators

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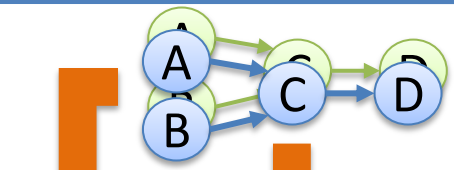

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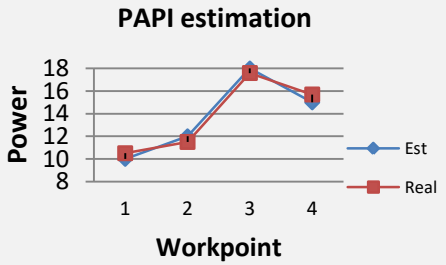
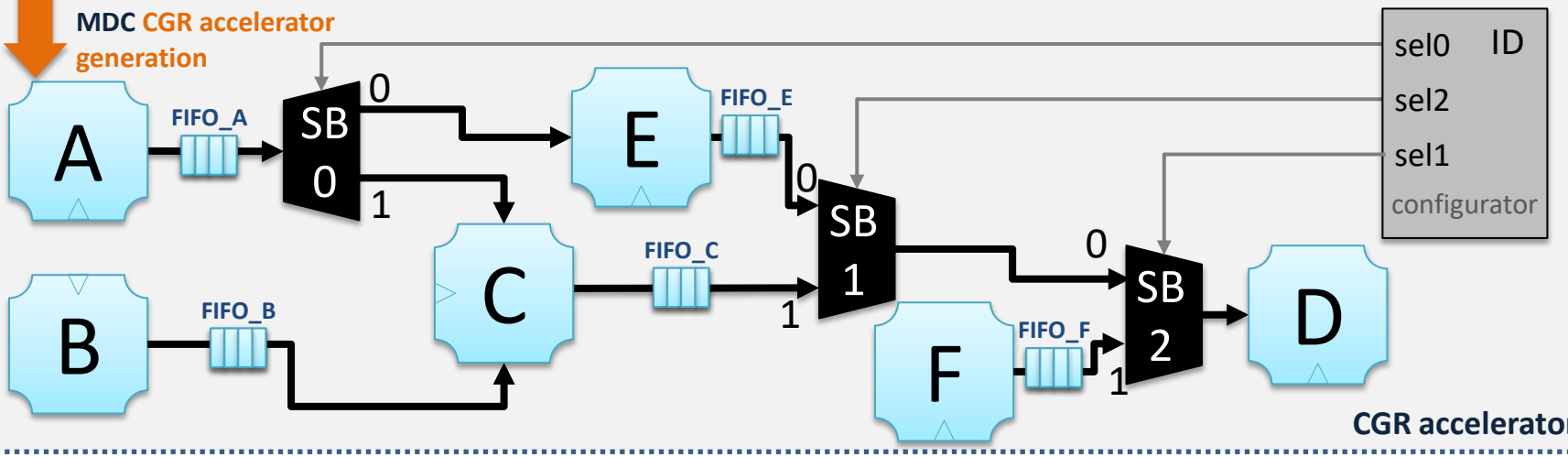


@run time

MDC CGR accelerator generation



CGR accelerator

Run-time Monitoring of CGR Accelerators

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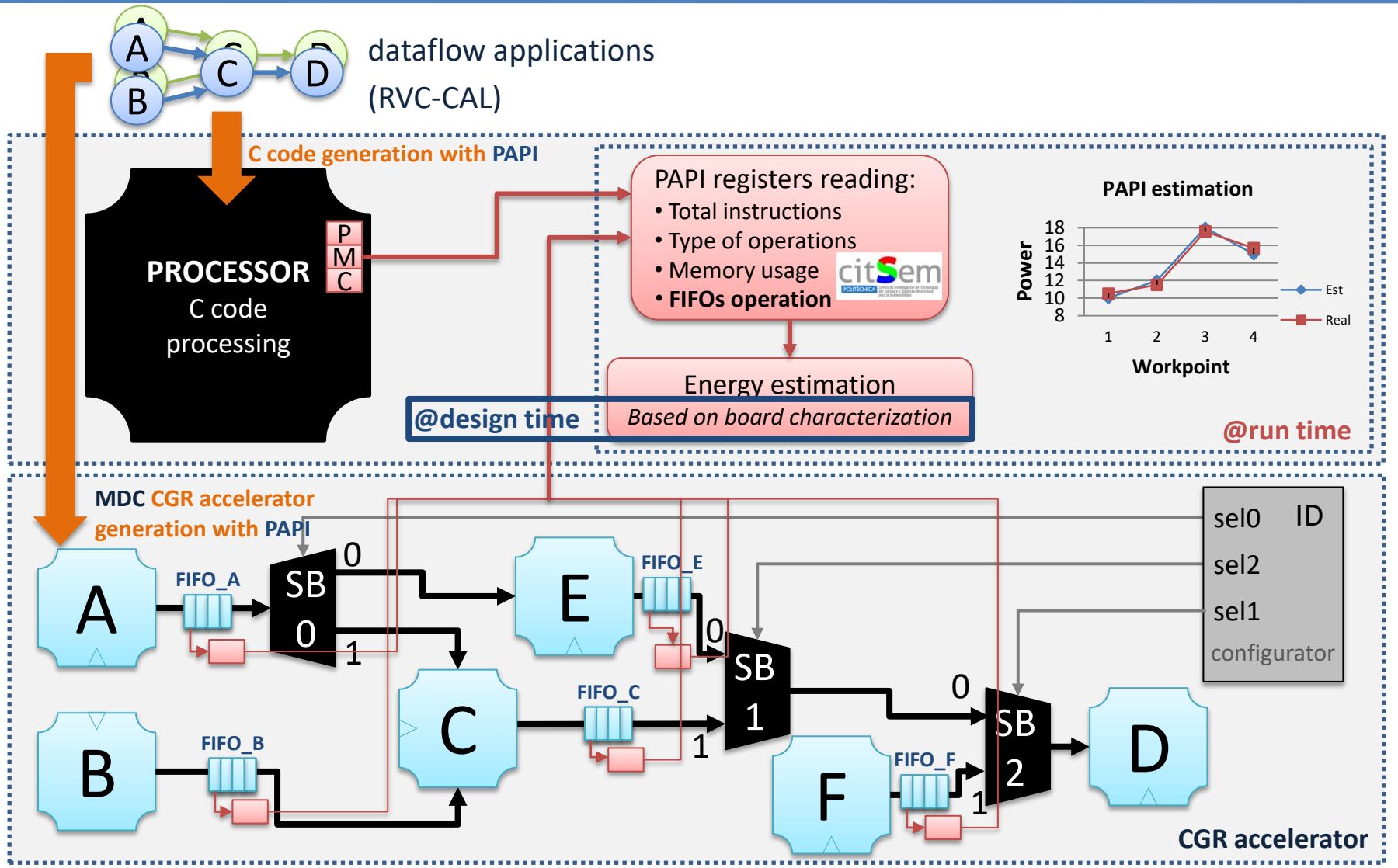

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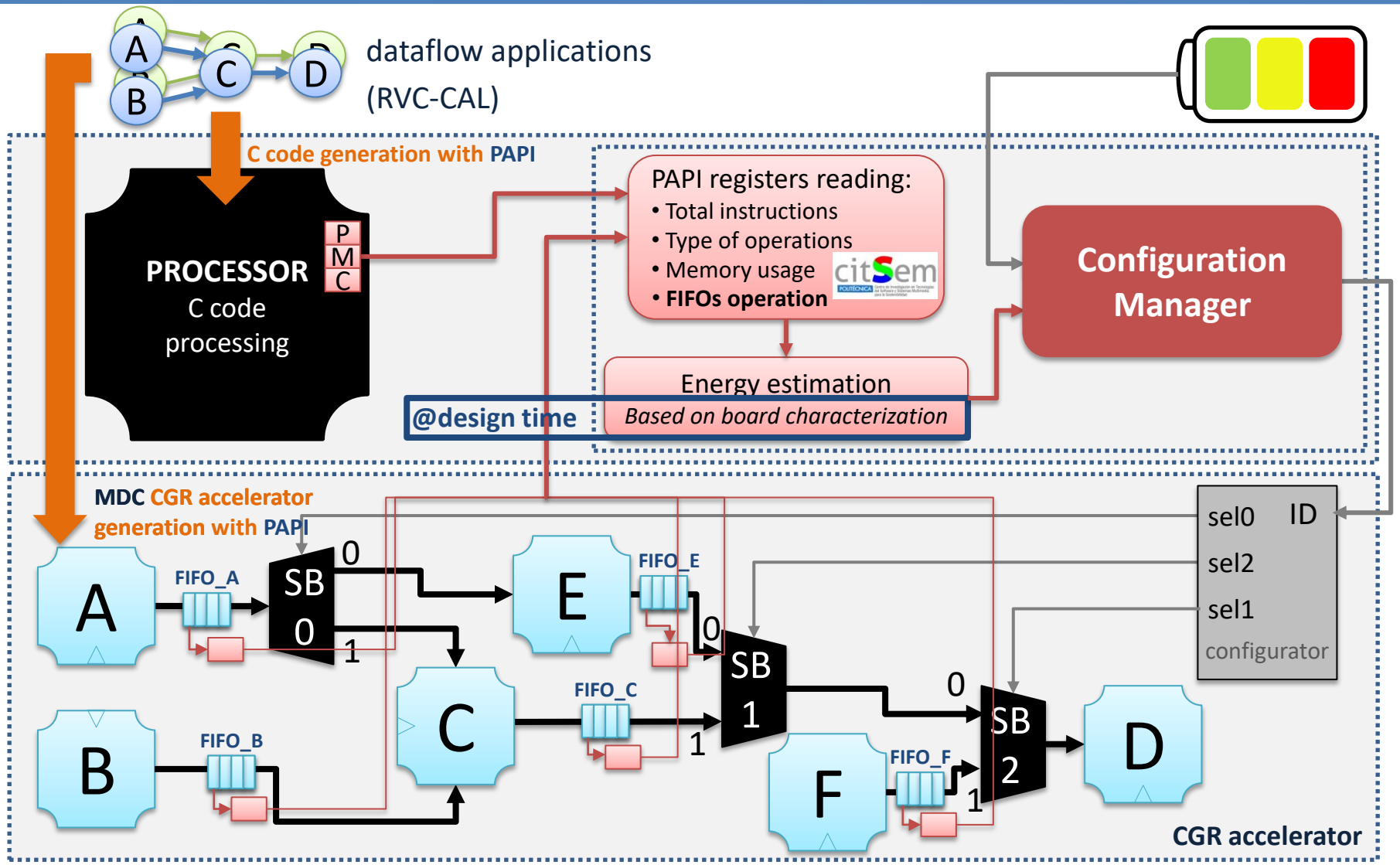

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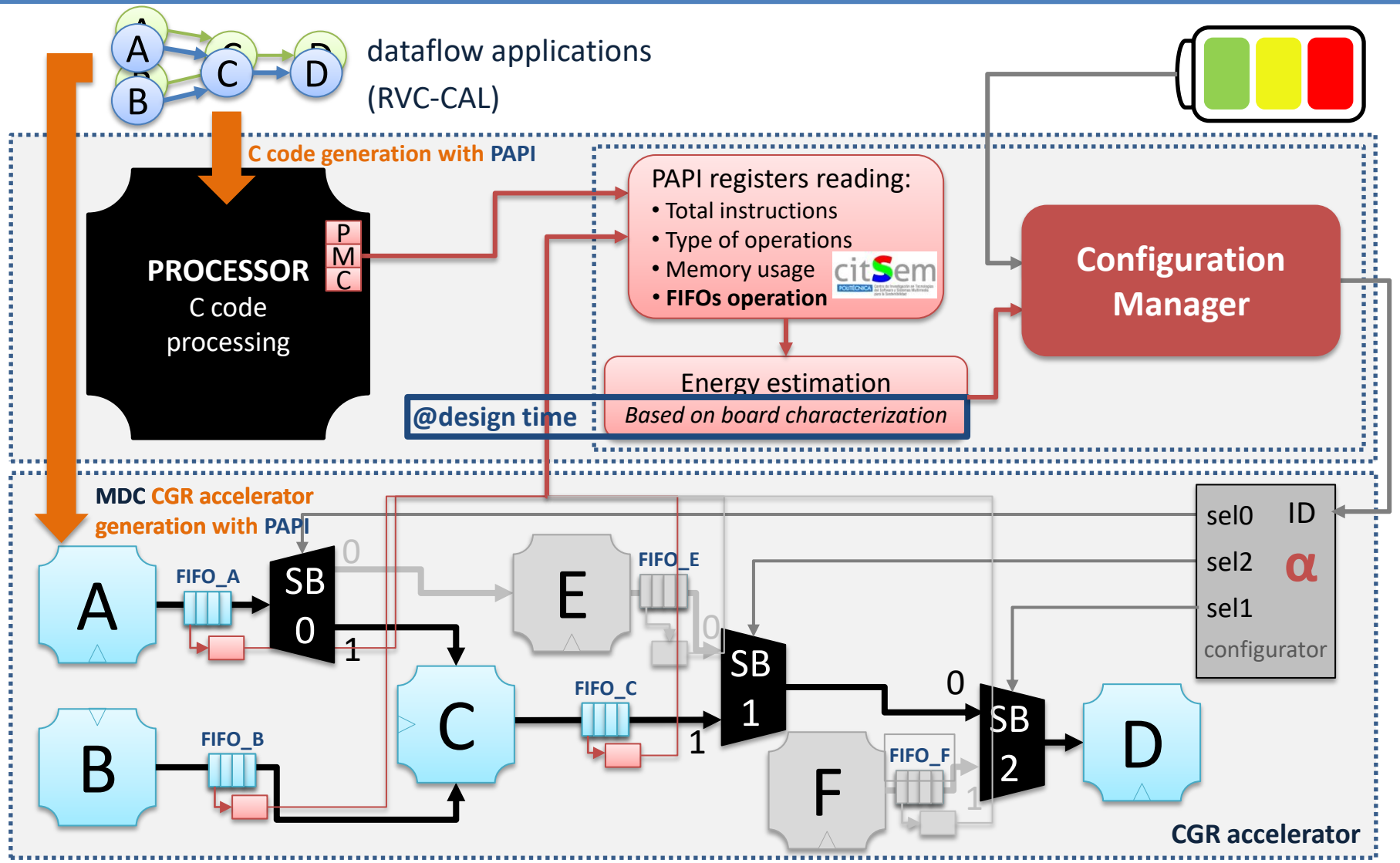

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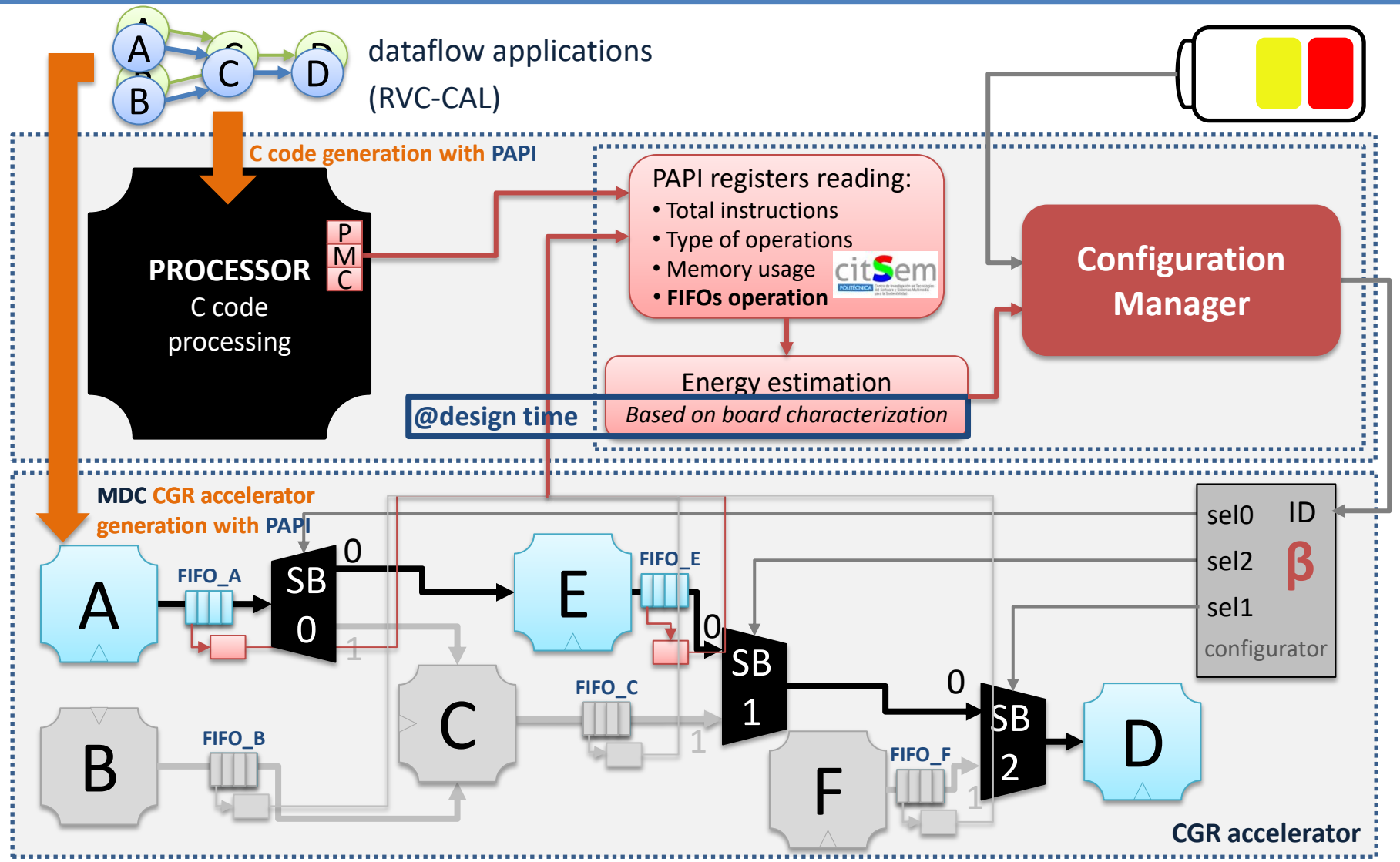

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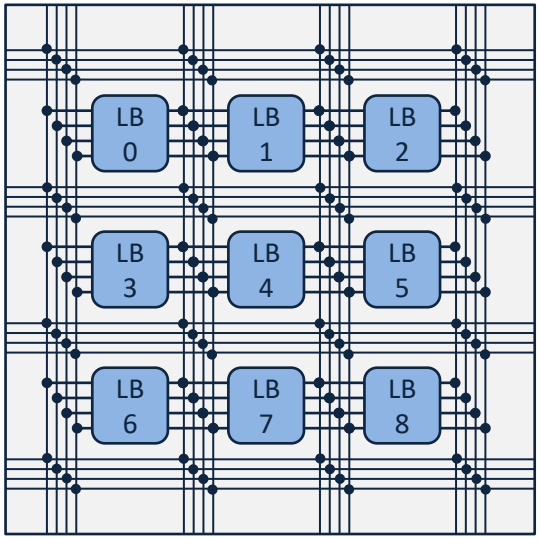
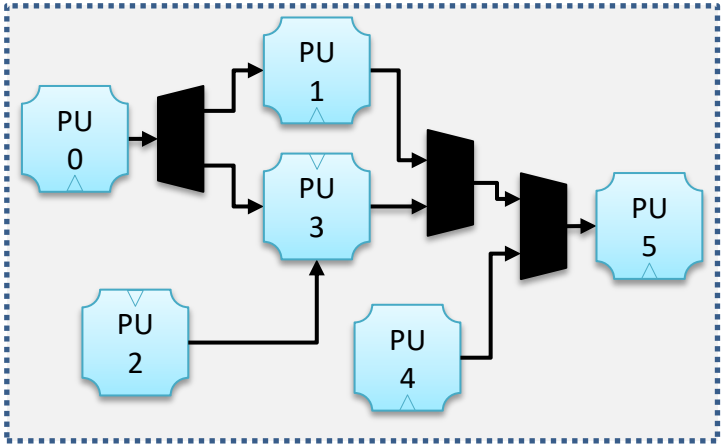
Providing Further Degrees of Reconfigurability

Fine-Grain and Partial Reconfiguration

FINE-GRAIN RECONFIGURATION (FPGA)



COARSE-GRAIN RECONFIGURATION (MDC ACCELERATOR)



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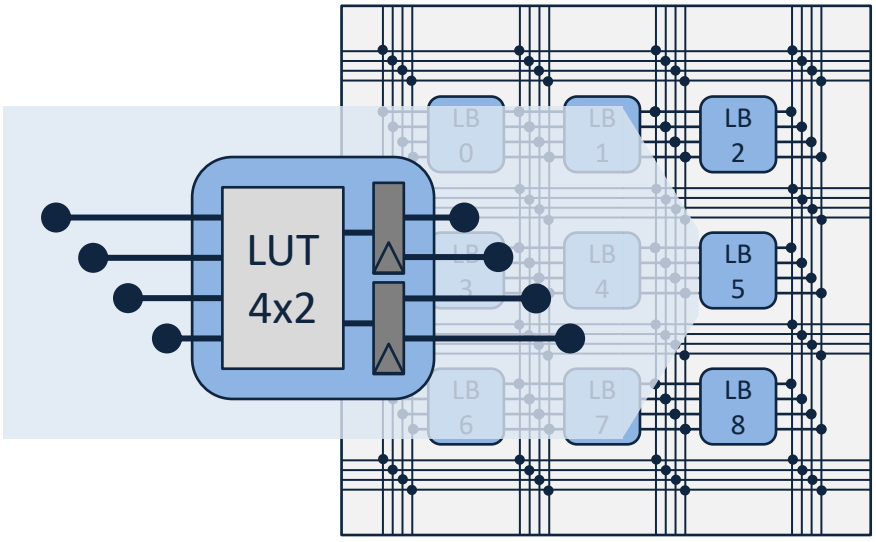

bit-level reconfiguration

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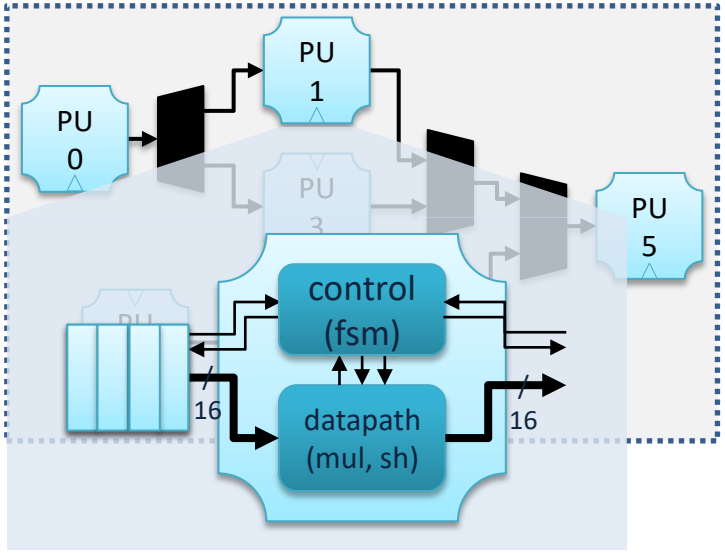

word-level reconfiguration

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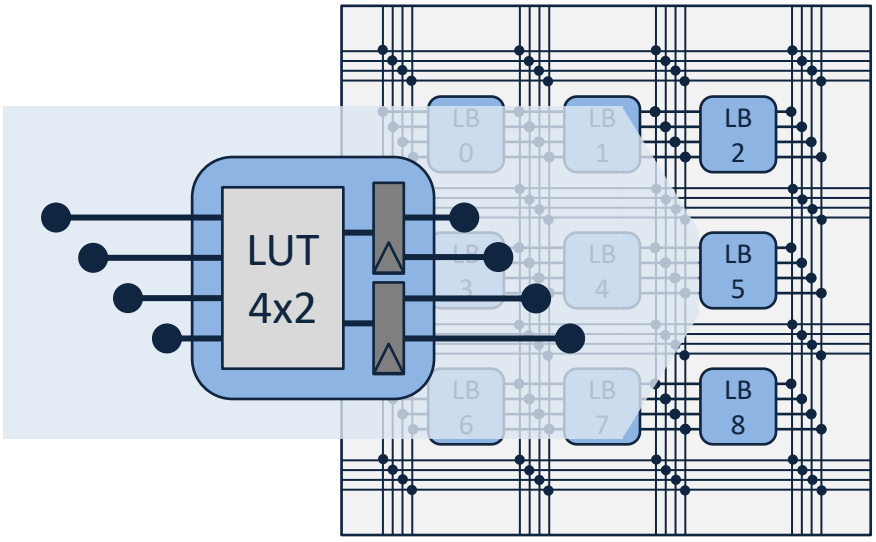

bit-level reconfiguration

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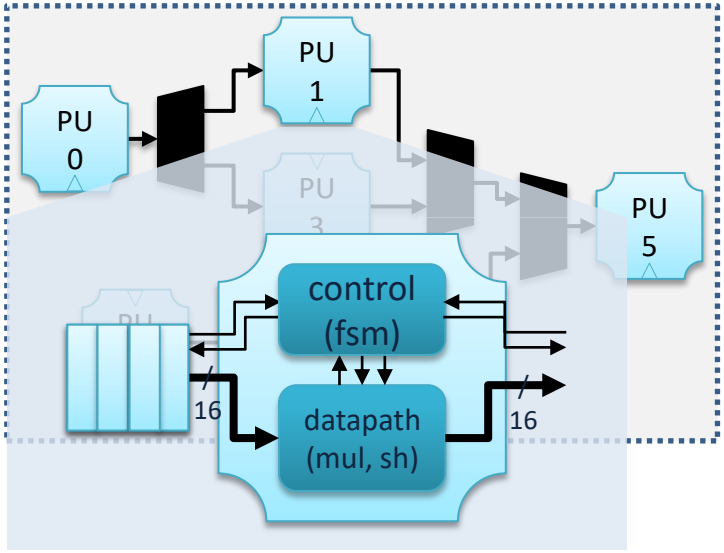

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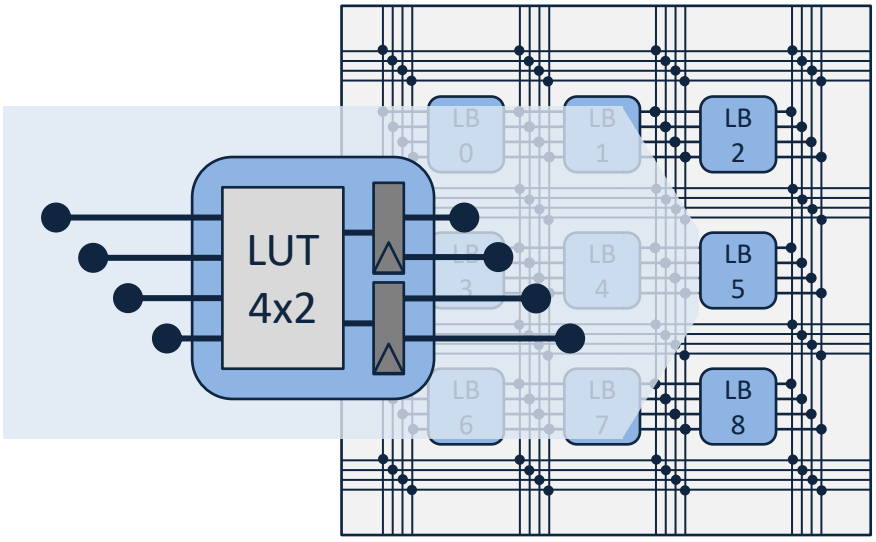

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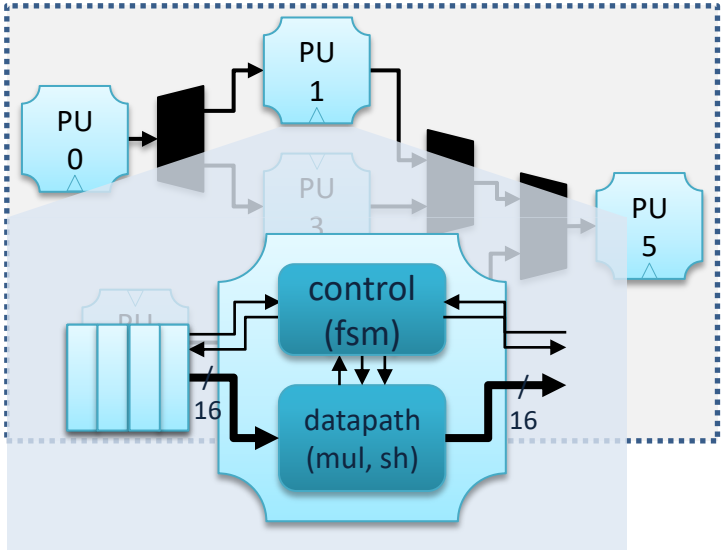

bit-level reconfiguration

very flexible (any kind of HDL defined system)

slow to configure (lot of switches and LUTs)

big memory footprint (long configuration bitstream)

word-level reconfiguration

small flexibility (fixed set of predefined configuration)

fast to configure (small amount of switches)

negligible memory footprint ($\log_2$(#config) bits)

Providing Further Degrees of Reconfigurability

Fine-Grain and Partial Reconfiguration

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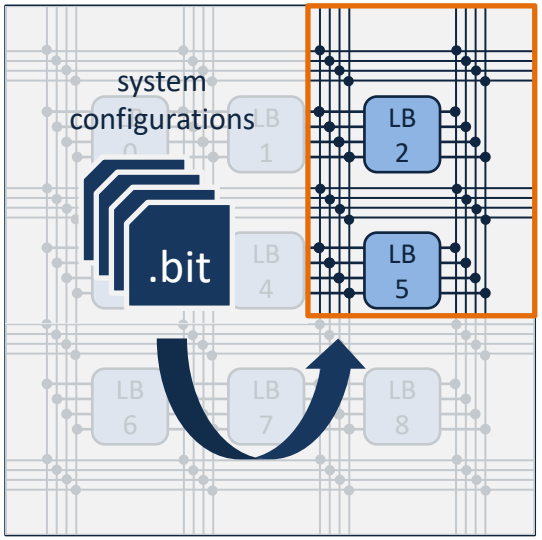
DYNAMIC PARTIAL RECONFIGURATION (DPR)
runtime reconfiguration of only a well defined region of the FPGA



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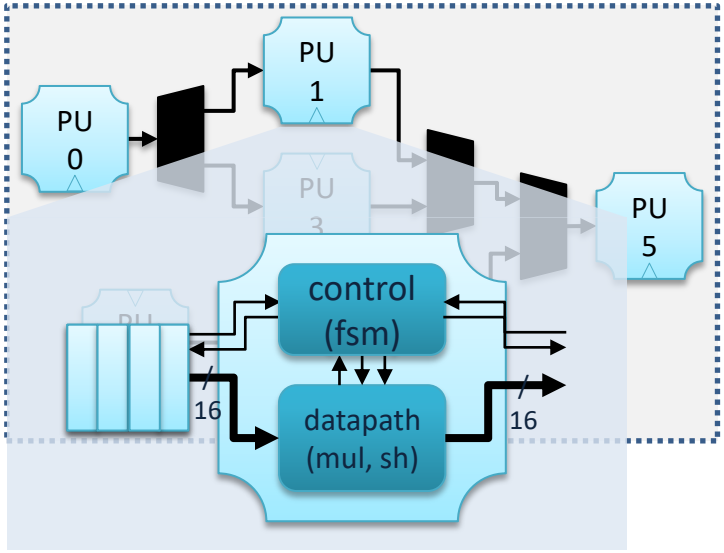

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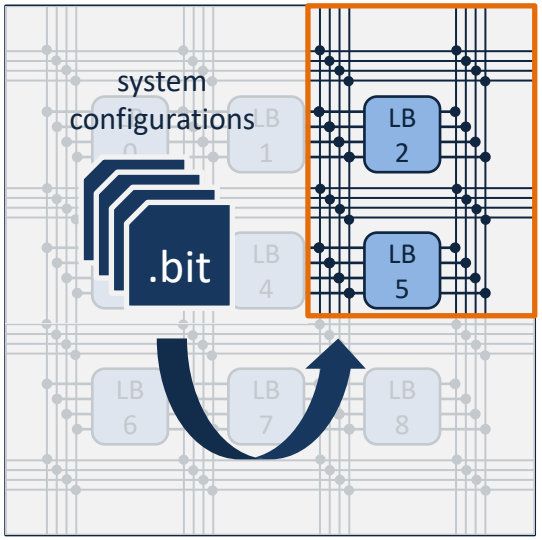

bit-level reconfiguration

flexible (HDL systems precedently implemented)

time to configure typically in terms of ms

memory footprint to be considered

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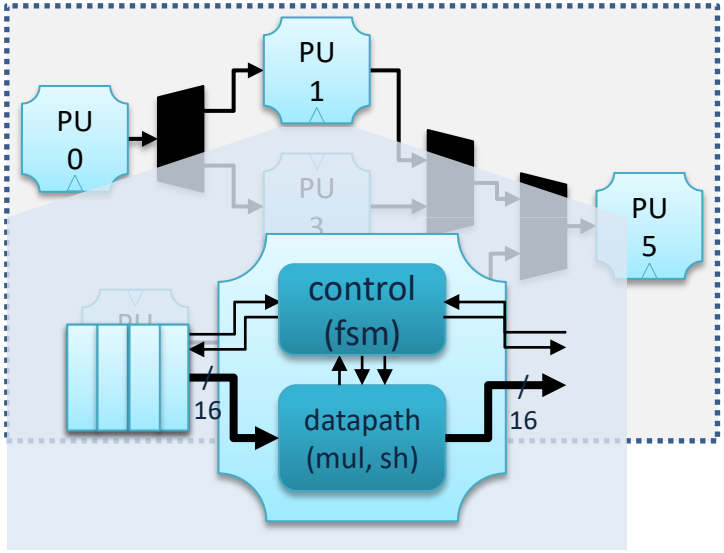

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Providing Further Degrees of Reconfigurability

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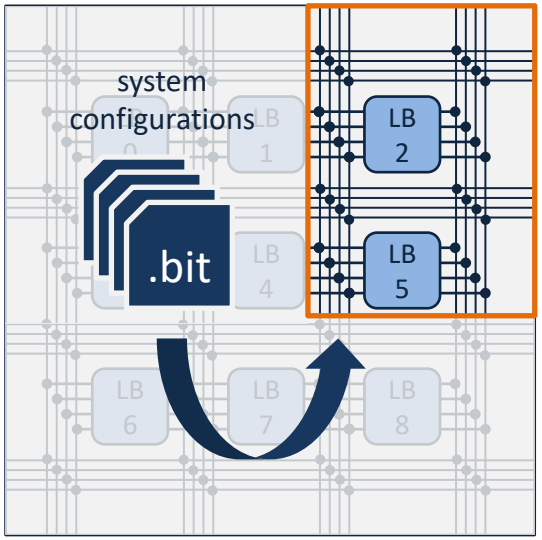

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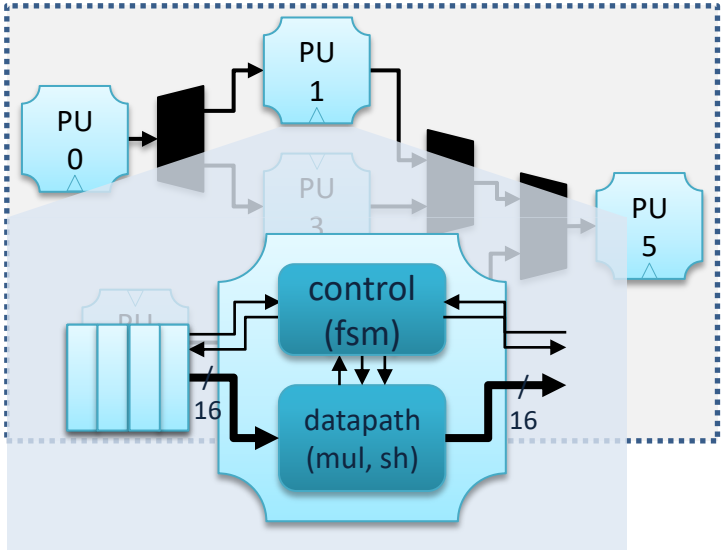

bit-level reconfiguration

flexible (HDL systems precedently implemented)

time to configure typically in terms of ms

memory footprint to be considered

power consumption peak during reconfiguration

word-level reconfiguration

small flexibility (fixed set of predefined configuration)

fast to configure (small amount of switches)

negligible memory footprint ($\log_2$(#config) bits)

power consumption due to reconfiguration

Providing Further Degrees of Reconfigurability

Fine-Grain and Partial Reconfiguration

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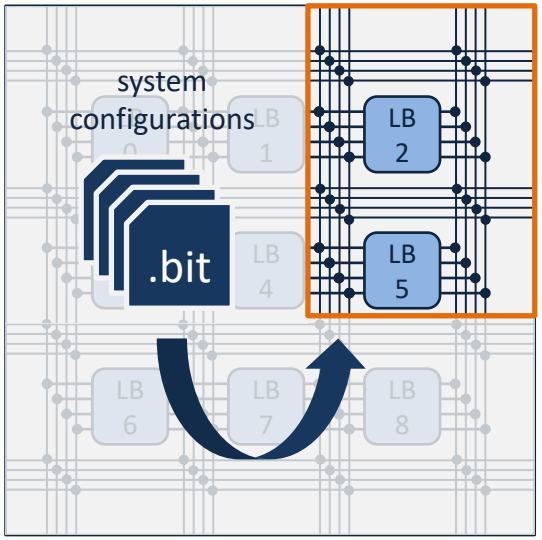

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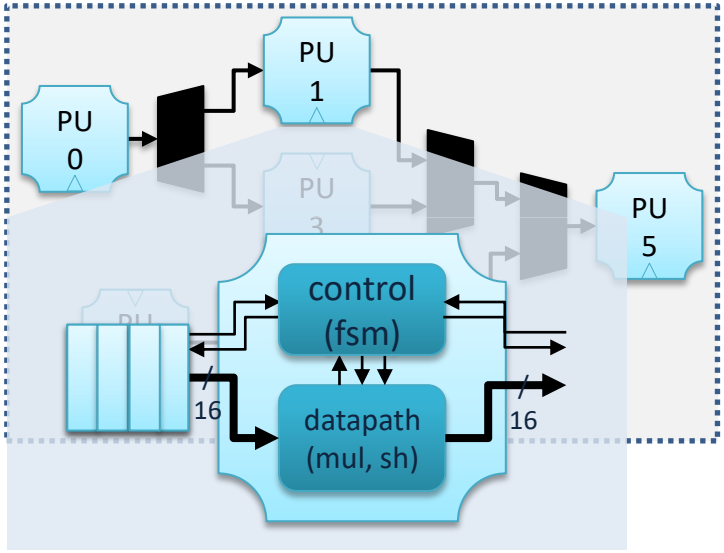


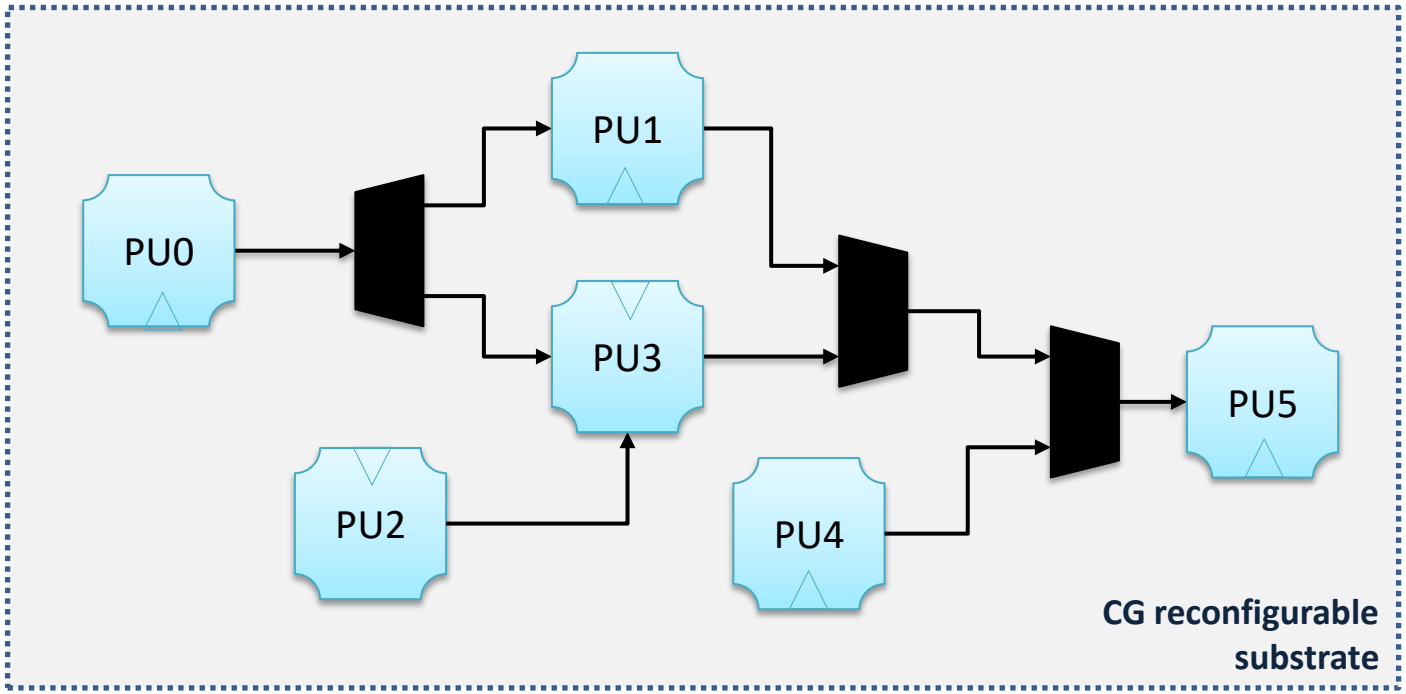
word-level reconfiguration

COMPLEMENTARITY

DPR	CGR
BIG change, BIG overhead	SMALL change, SMALL overhead

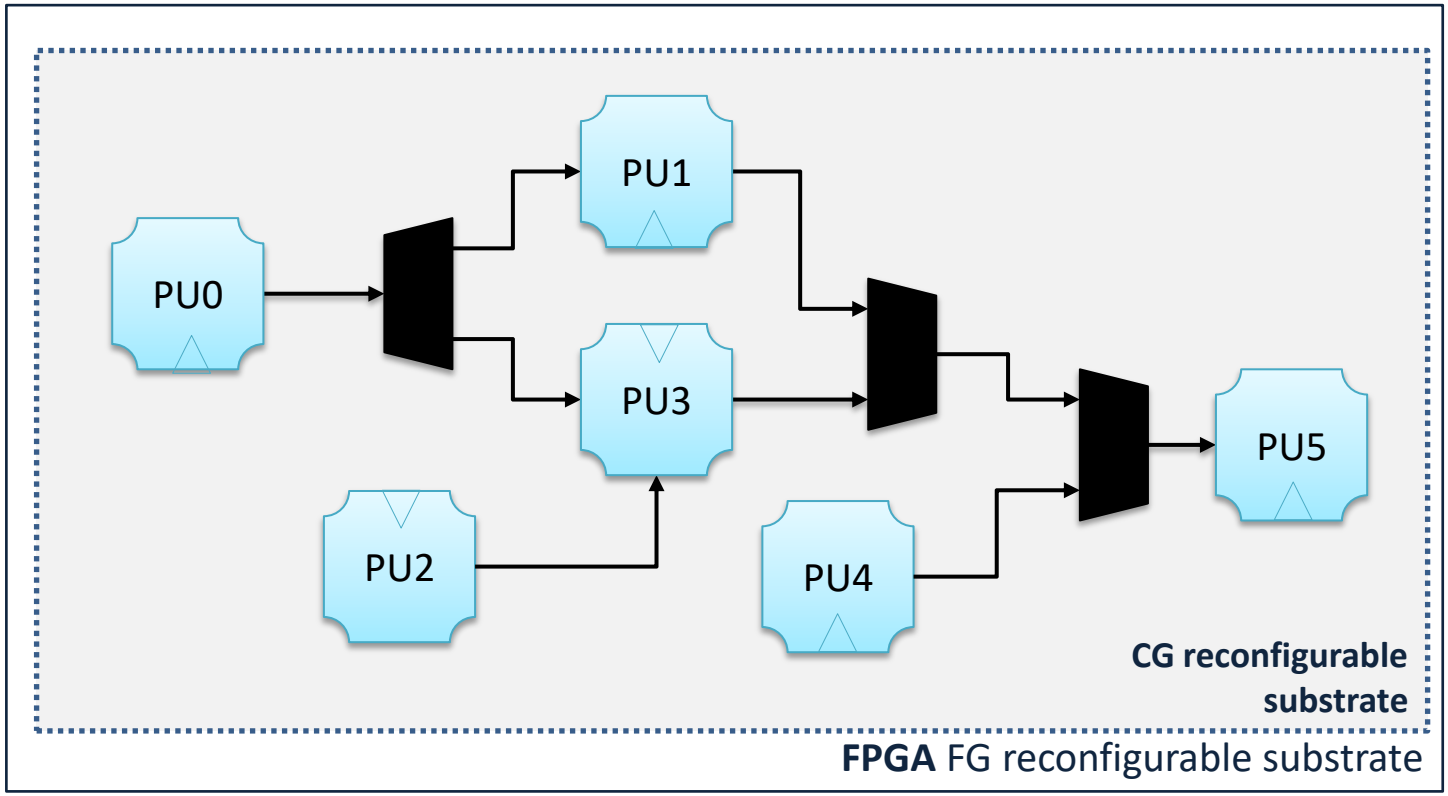
Providing Further Degrees of Reconfigurability

FG into CG reconfiguration



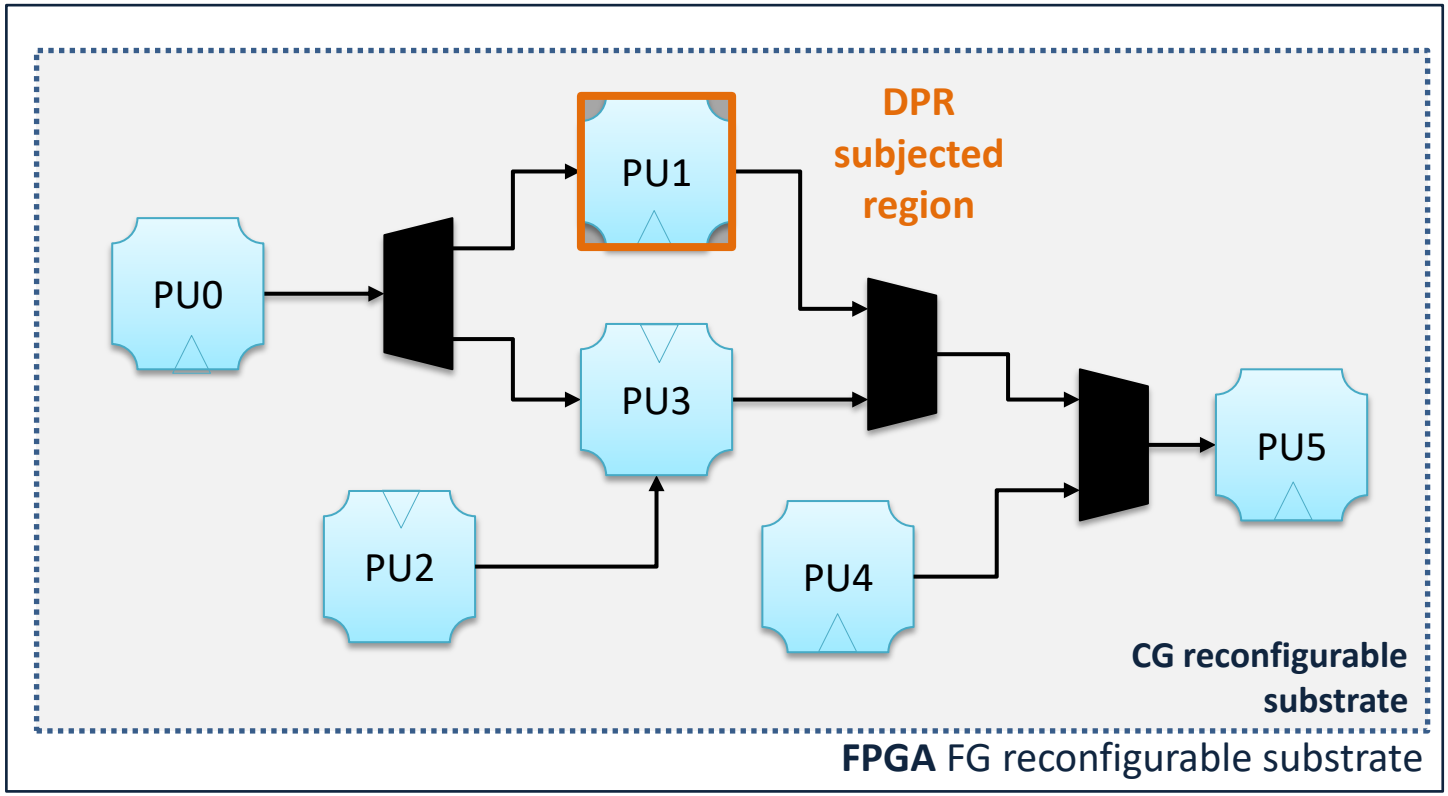
Providing Further Degrees of Reconfigurability

FG into CG reconfiguration



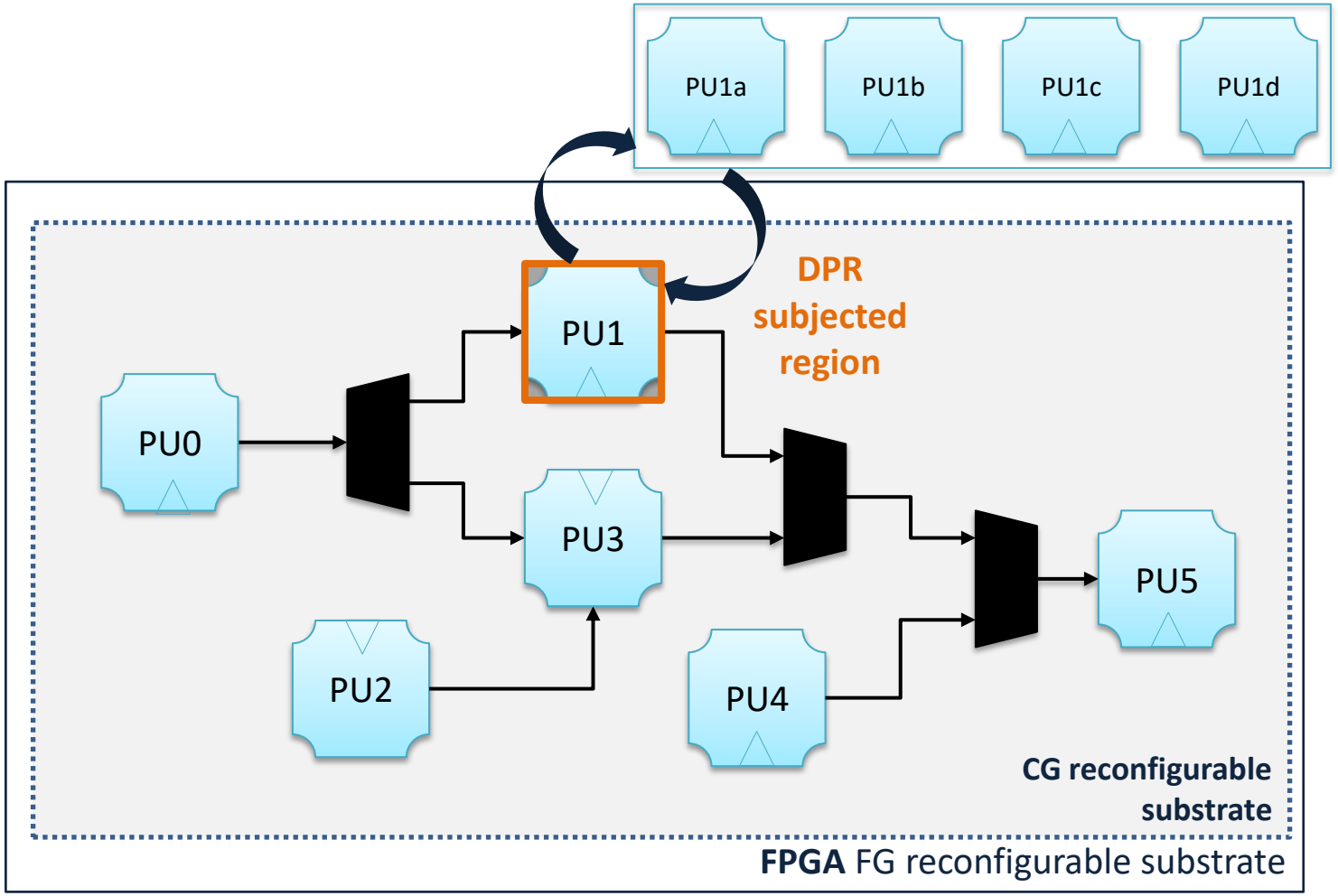
Providing Further Degrees of Reconfigurability

FG into CG reconfiguration



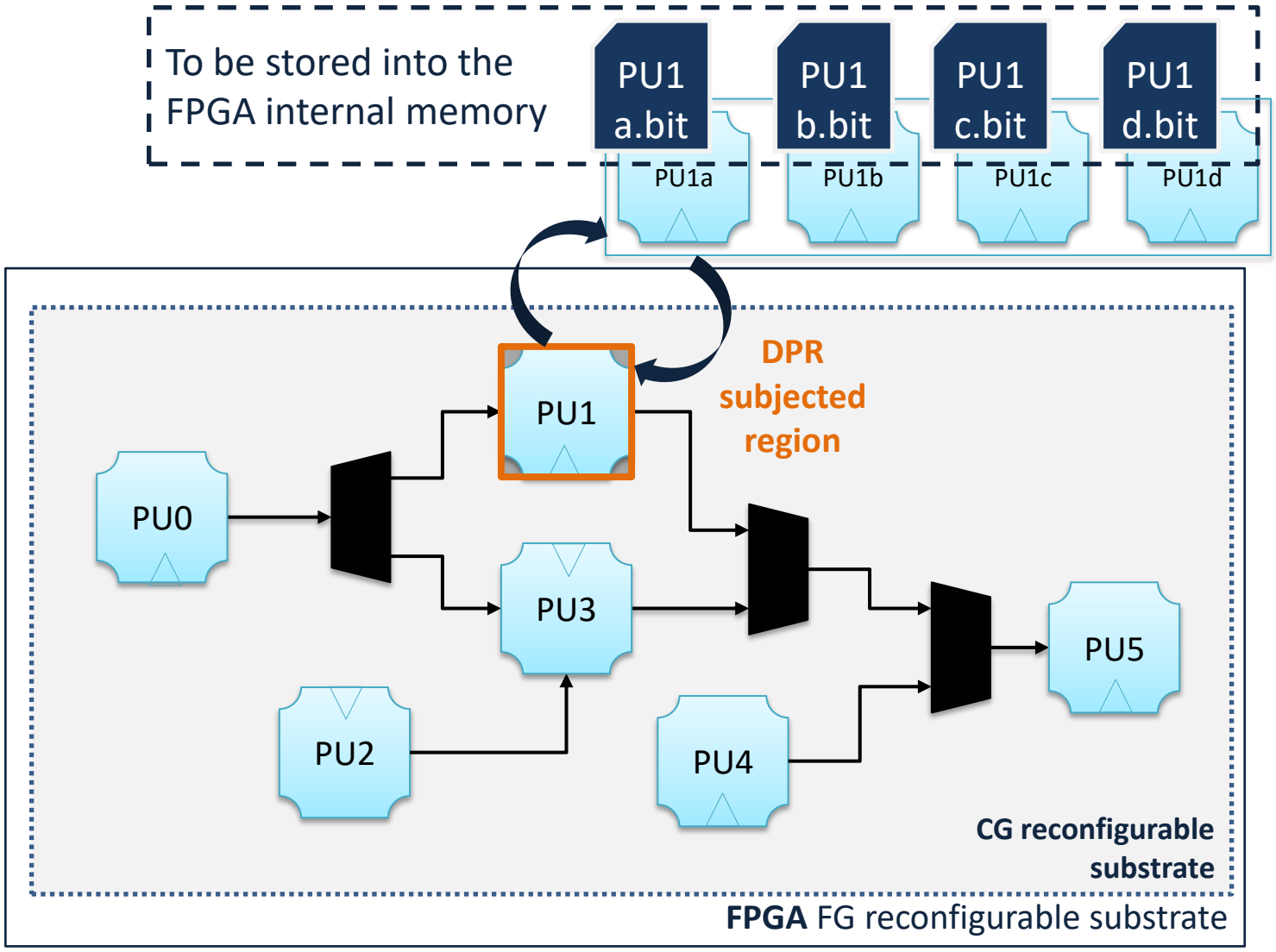
Providing Further Degrees of Reconfigurability

FG into CG reconfiguration



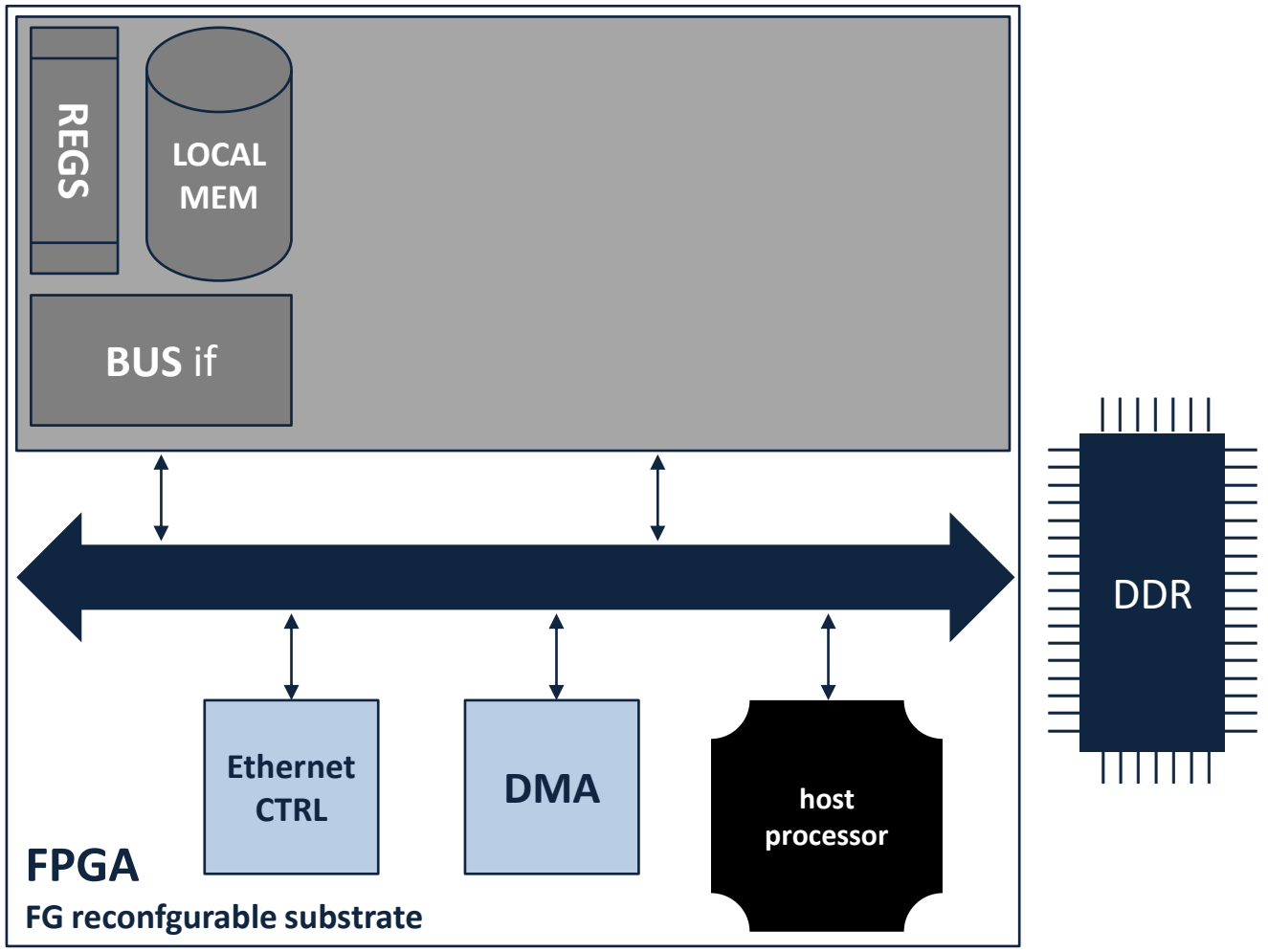
Providing Further Degrees of Reconfigurability

FG into CG reconfiguration



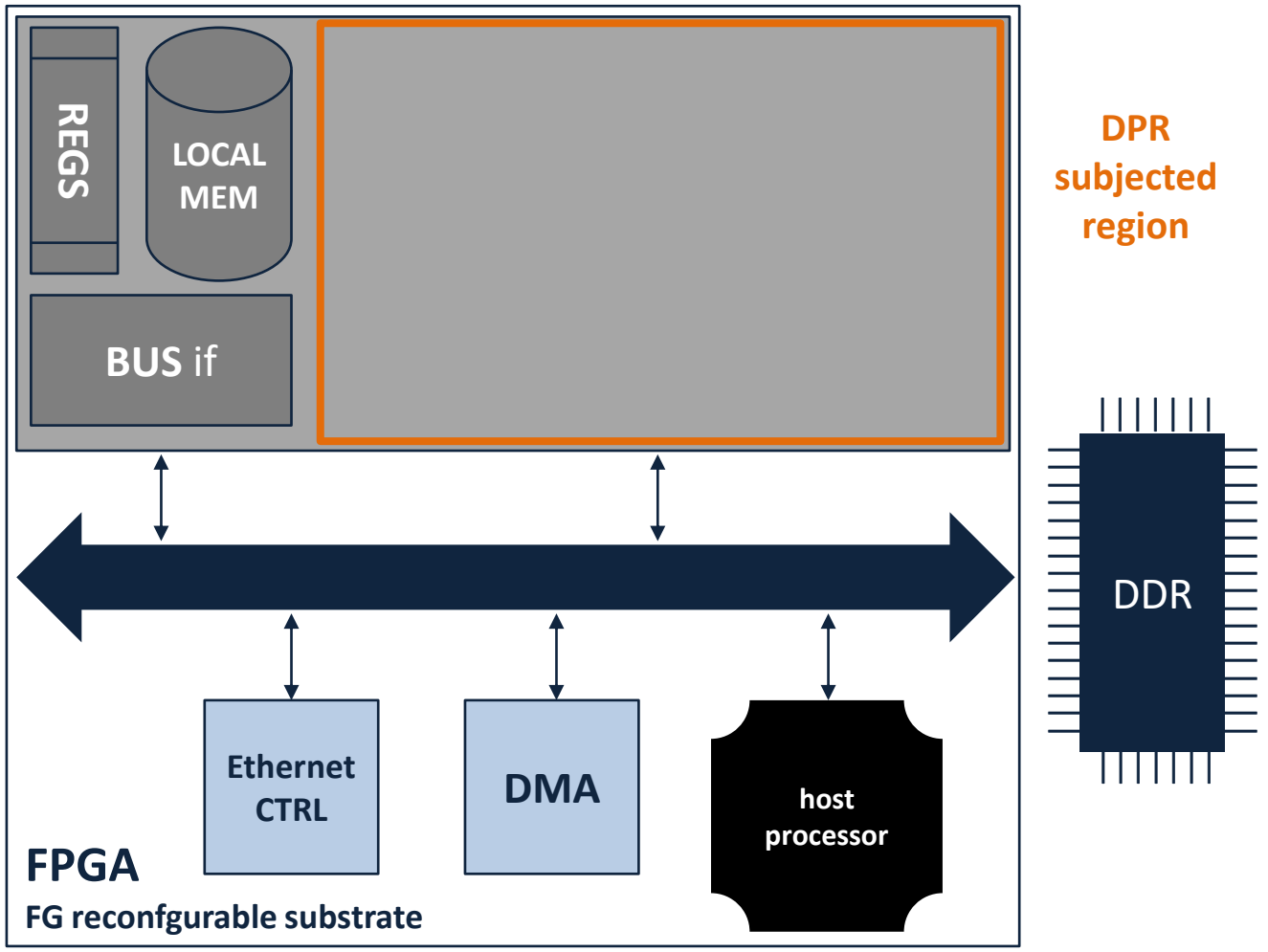
Providing Further Degrees of Reconfigurability

CG into FG reconfiguration



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

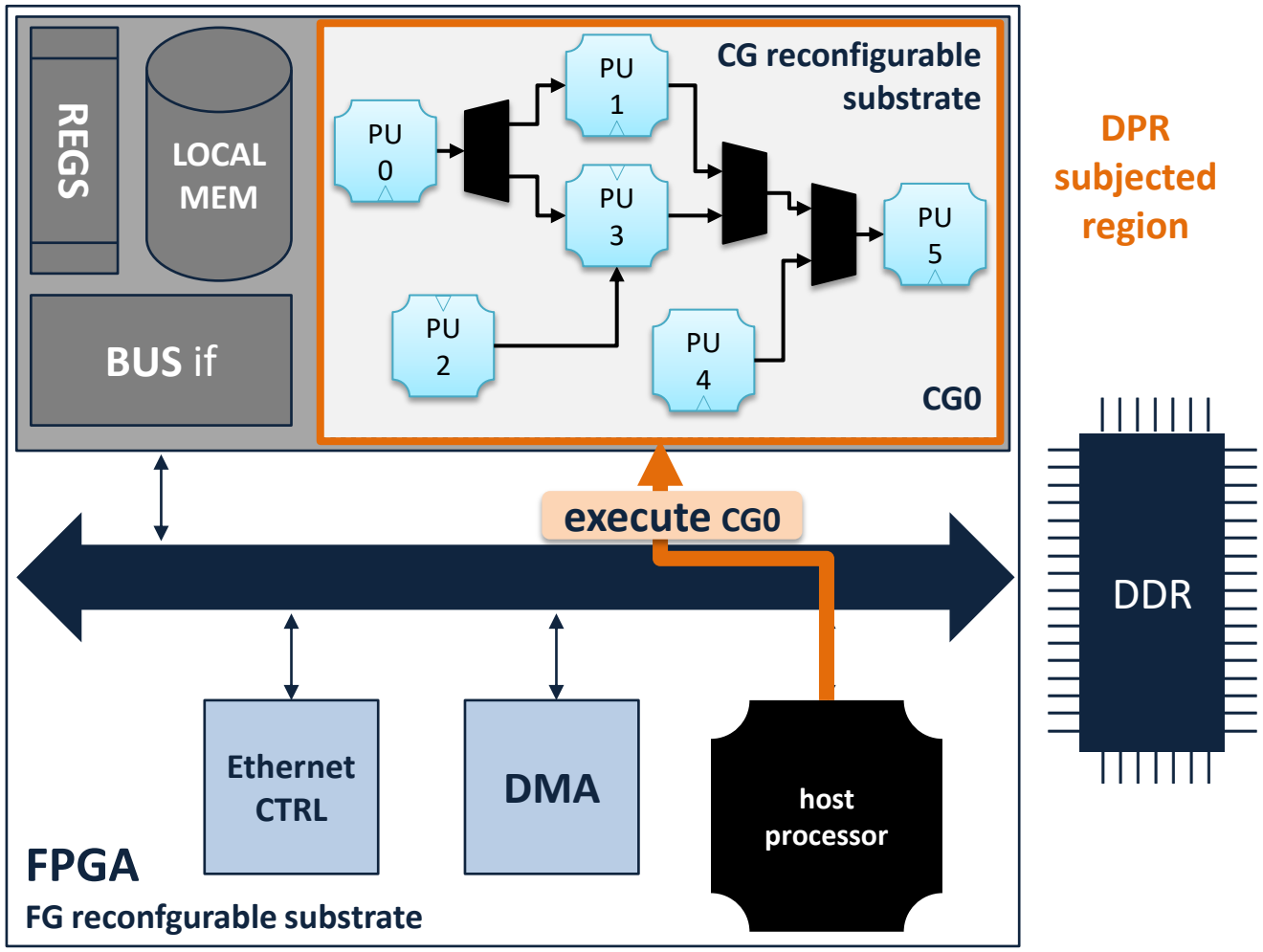


Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0



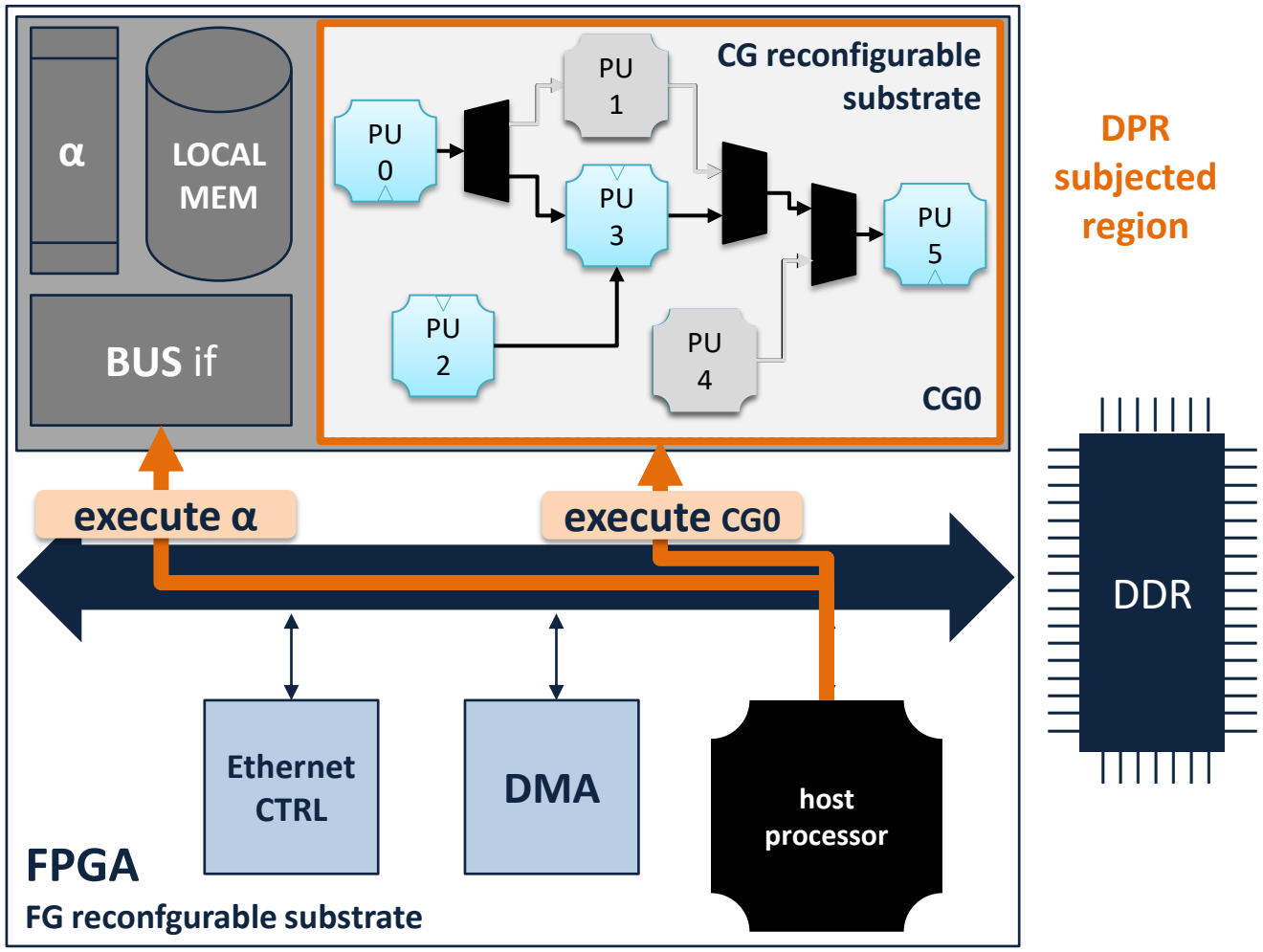
Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

t1: config CG = α



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

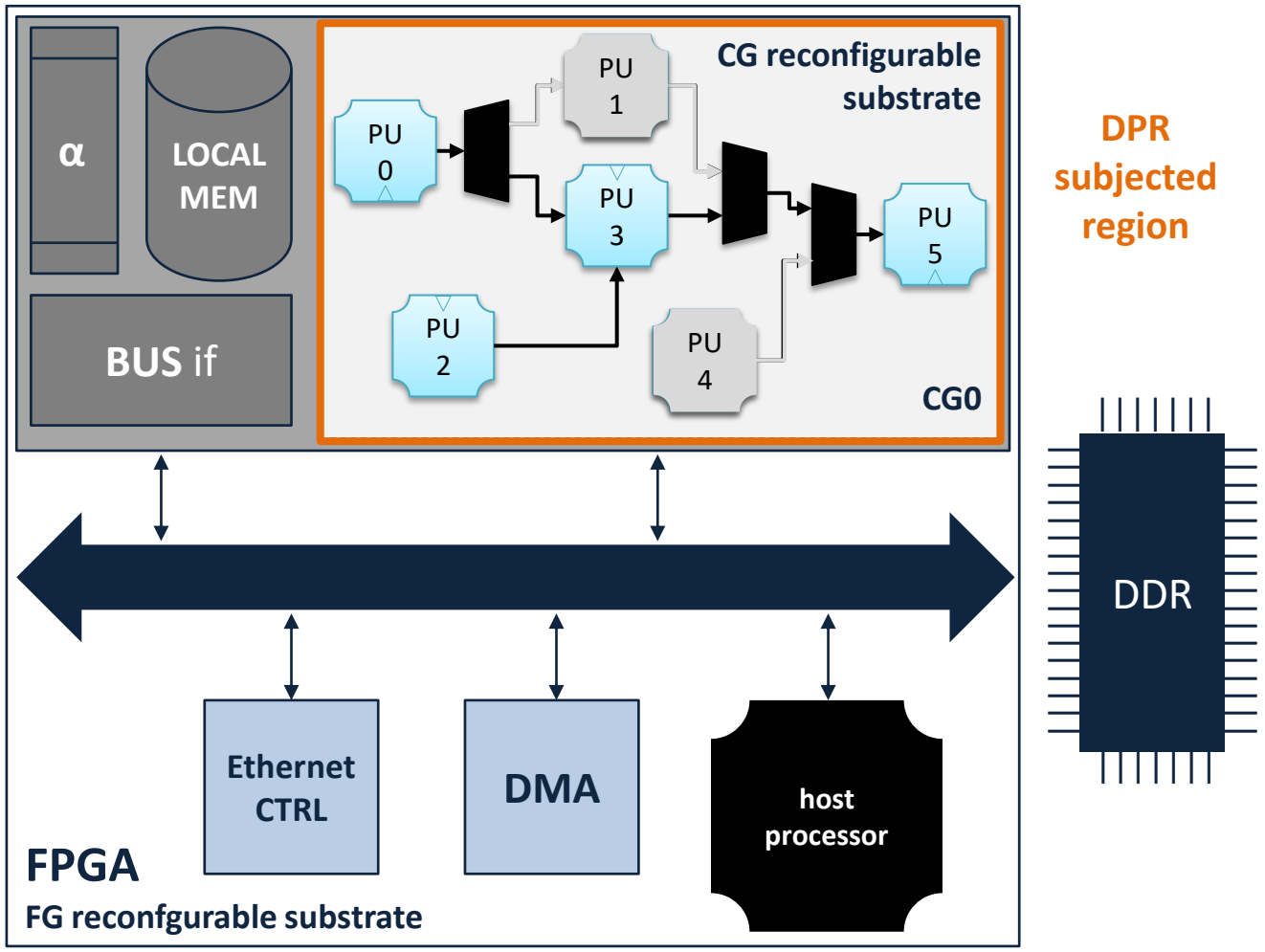
t0: config FG = CG0

t1: config CG = α

…

SMALL context change

…



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

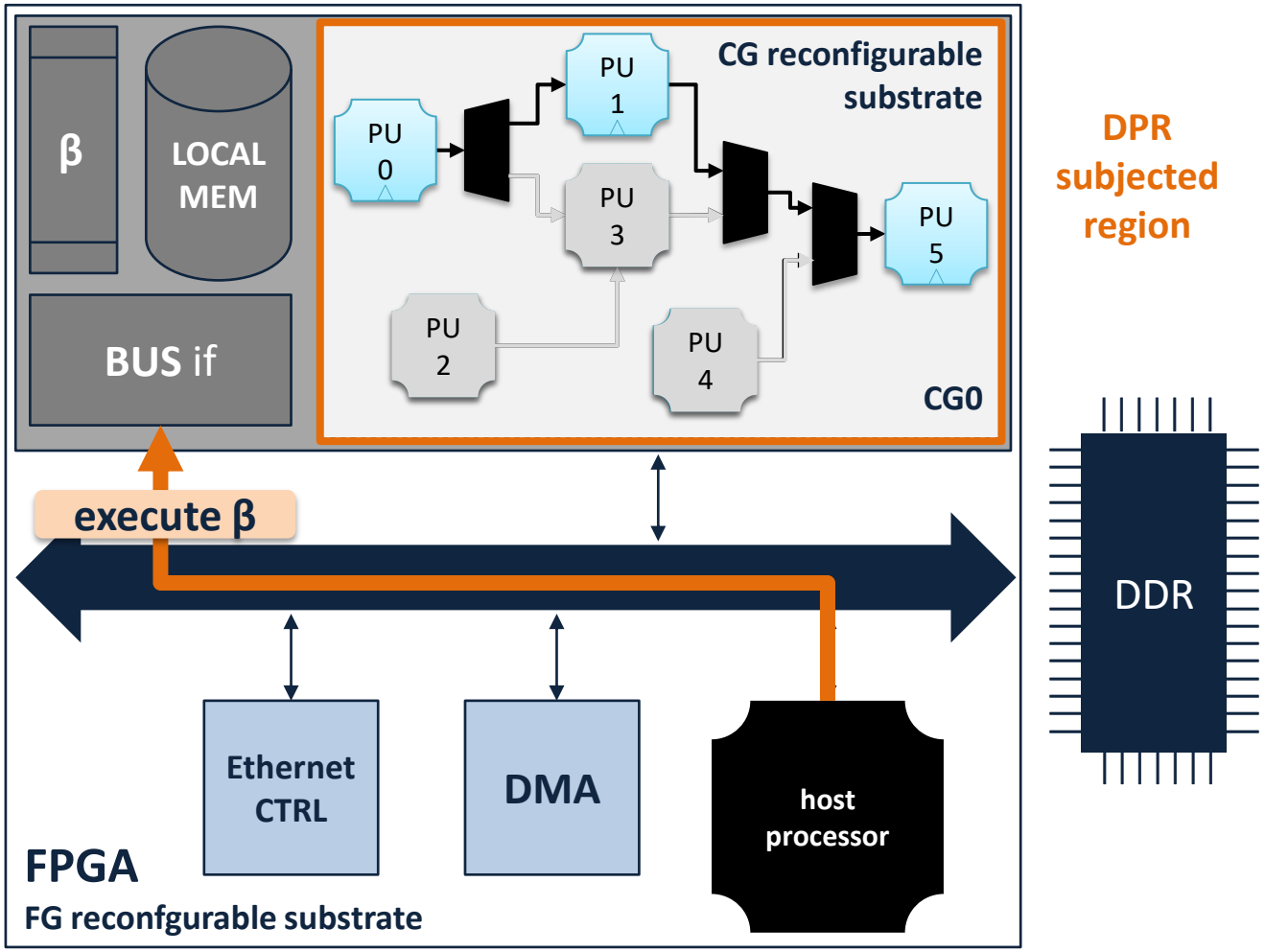
t1: config CG = α

…

SMALL context change

…

t2: config CG = β



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

t1: config CG = α

…

SMALL context change

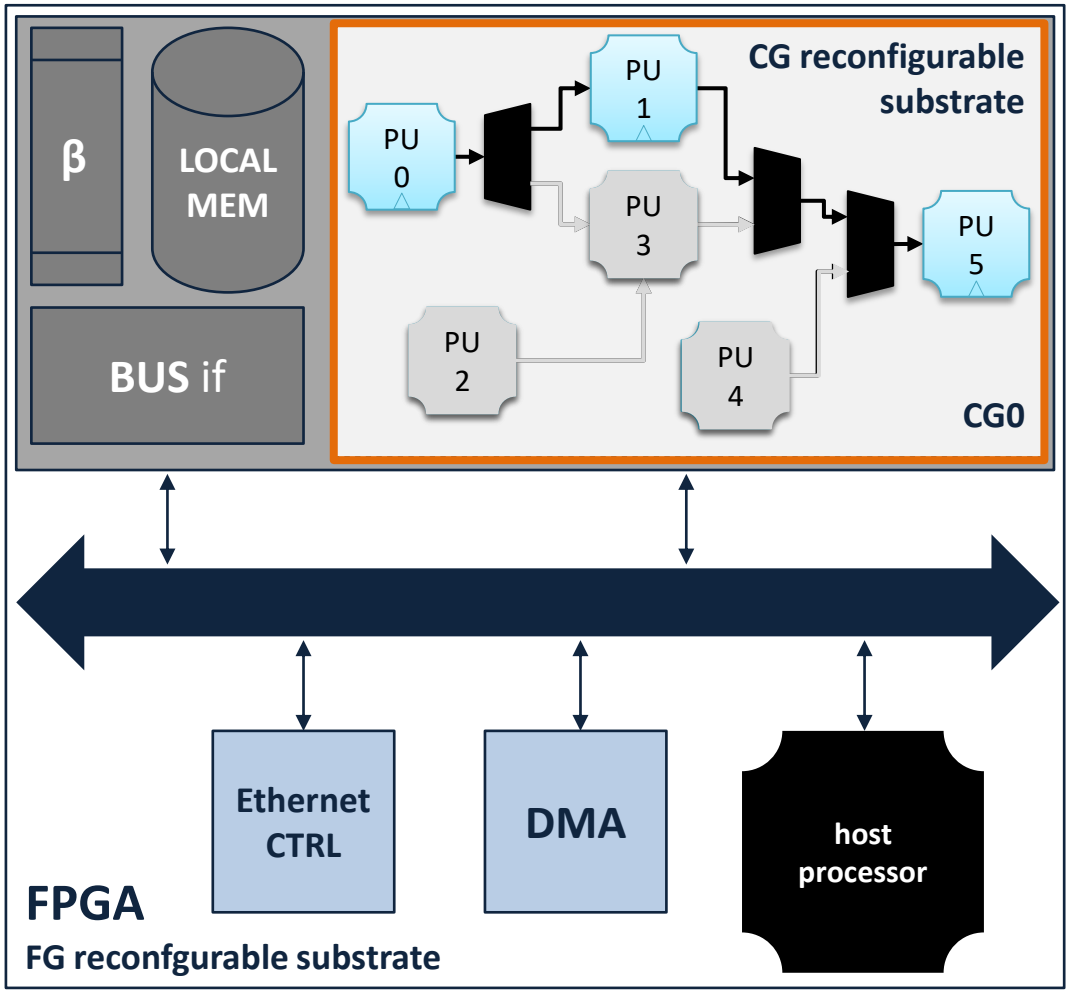
…

t2: config CG = β

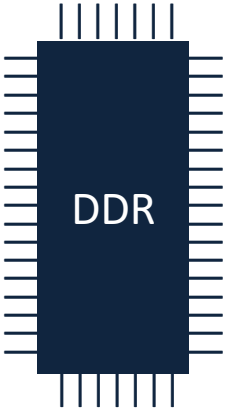
…

SMALL context change

…



DPR subjected region



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

t1: config CG = α

…

SMALL context change

…

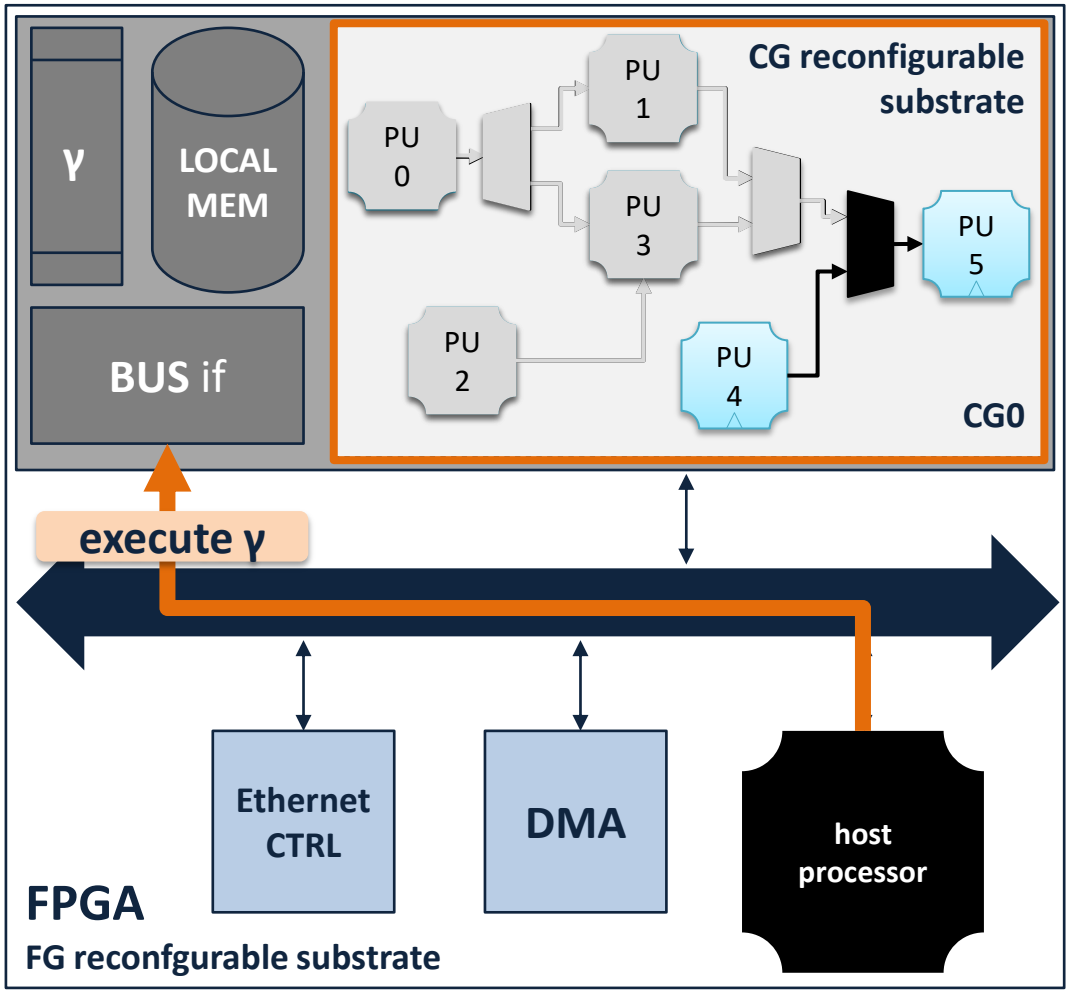
t2: config CG = β

…

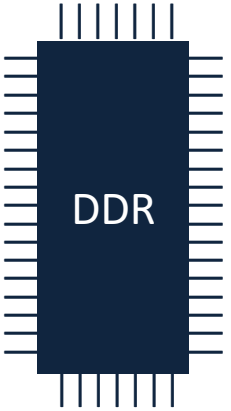
SMALL context change

…

t3: config CG = γ



DPR subjected region



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

t1: config CG = α

…

SMALL context change

…

t2: config CG = β

…

SMALL context change

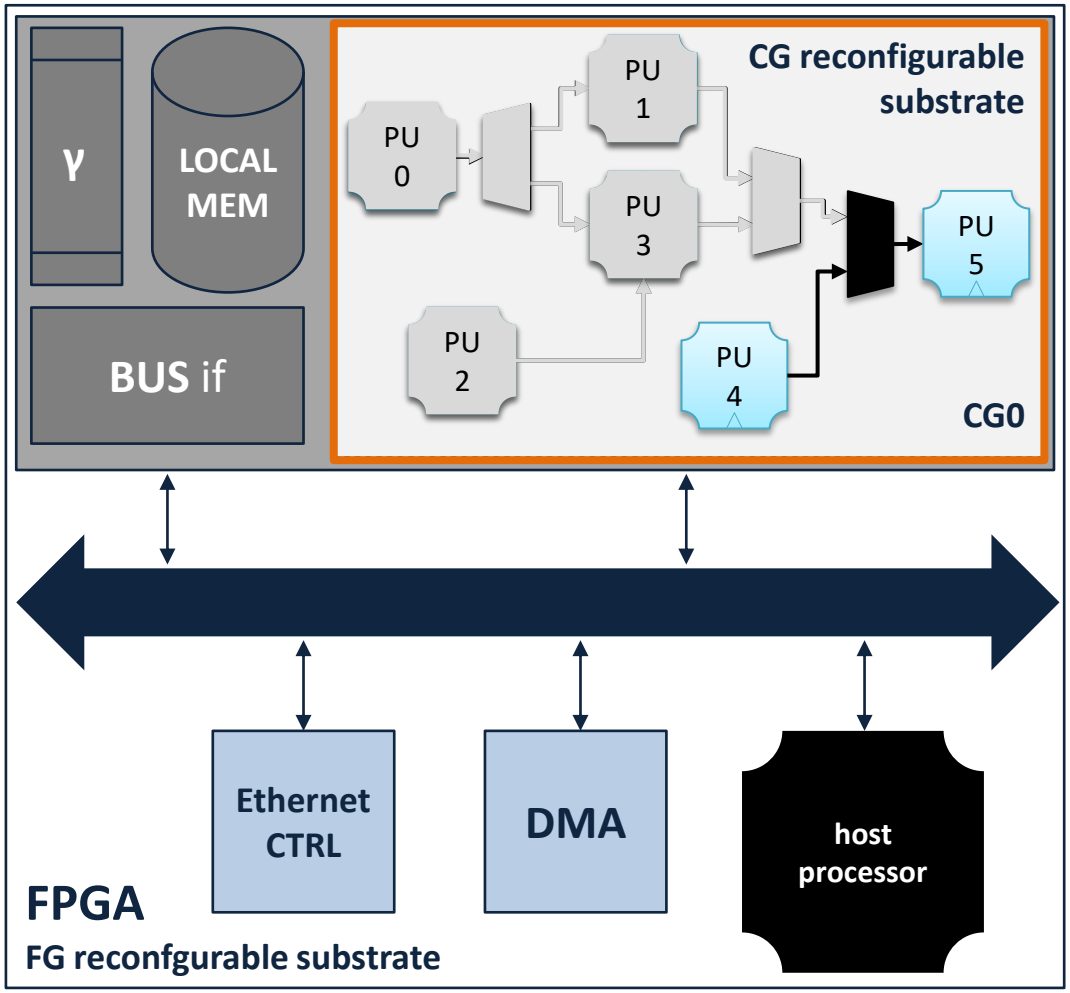
…

t3: config CG = γ

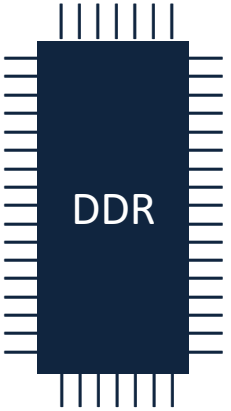
…

BIG context change

…



DPR subjected region



Providing Further Degrees of Reconfigurability

CG into FG reconfiguration

RUNTIME:

t0: config FG = CG0

t1: config CG = α

…

SMALL context change

…

t2: config CG = β

…

SMALL context change

…

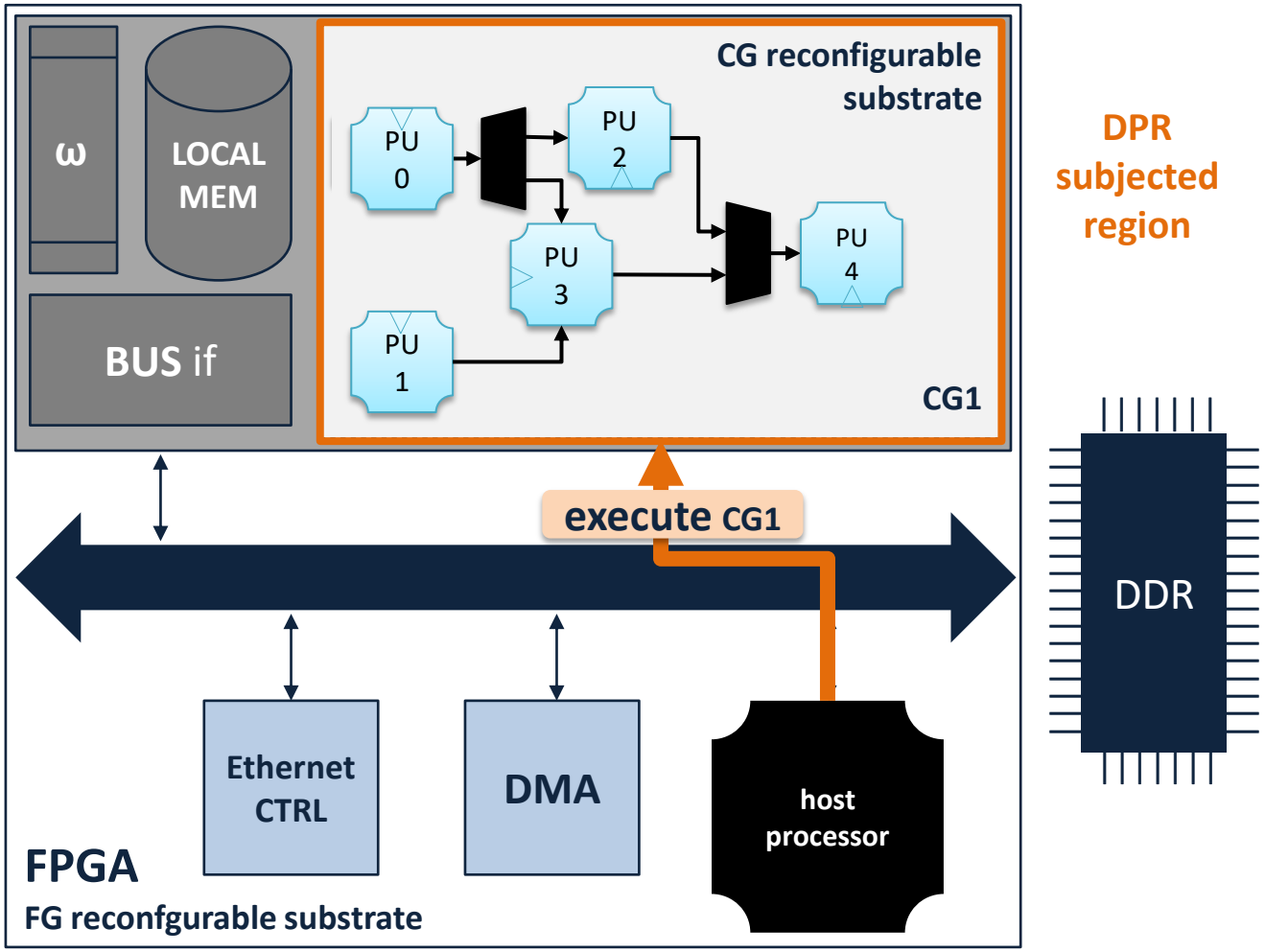
t3: config CG = γ

…

BIG context change

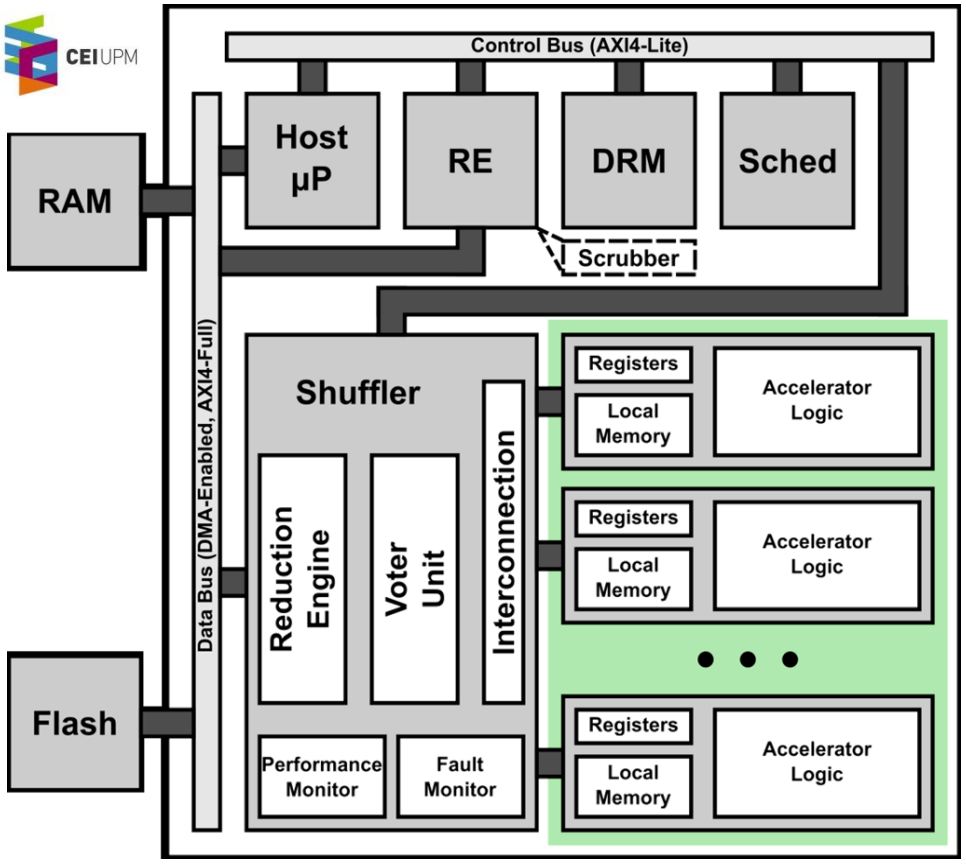
…

t4: config FG = CG1



Providing Further Degrees of Reconfigurability

CG into Artico^3

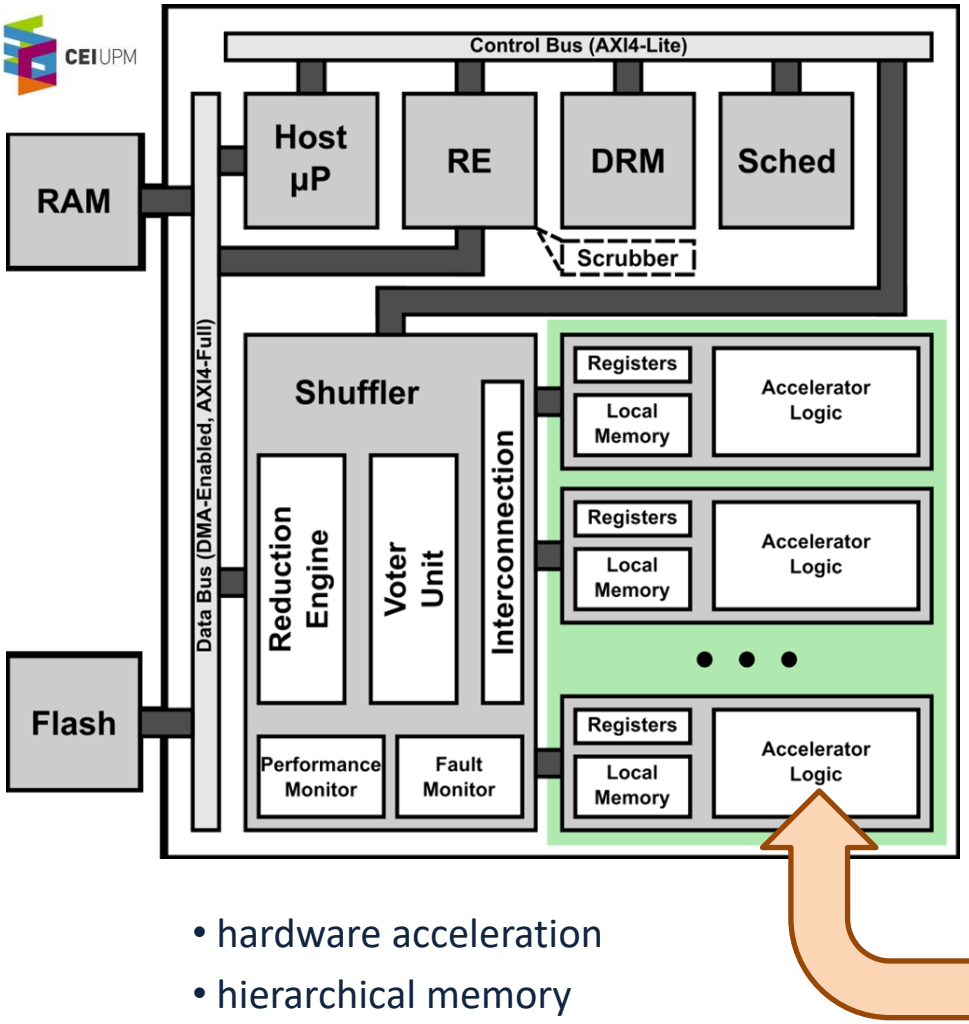


Artico3 is a **DPR** supporting architecture in charge of smartly manage **performance**, **consumption** and **dependability**.

- hardware acceleration
- hierarchical memory
- bus based, DMA enabled communication

Providing Further Degrees of Reconfigurability

CG into Artico^3



Artico3 is a **DPR** supporting architecture in charge of smartly manage **performance**, **consumption** and **dependability**.

- enhance **flexibility** by enabling CGR within Artico3 slots

- hardware acceleration
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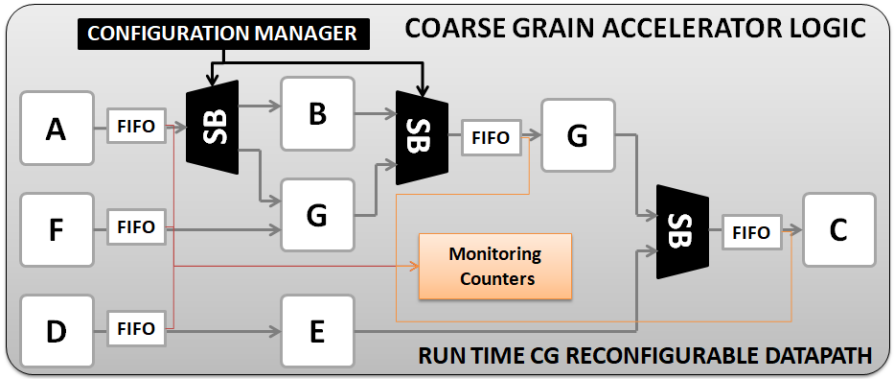
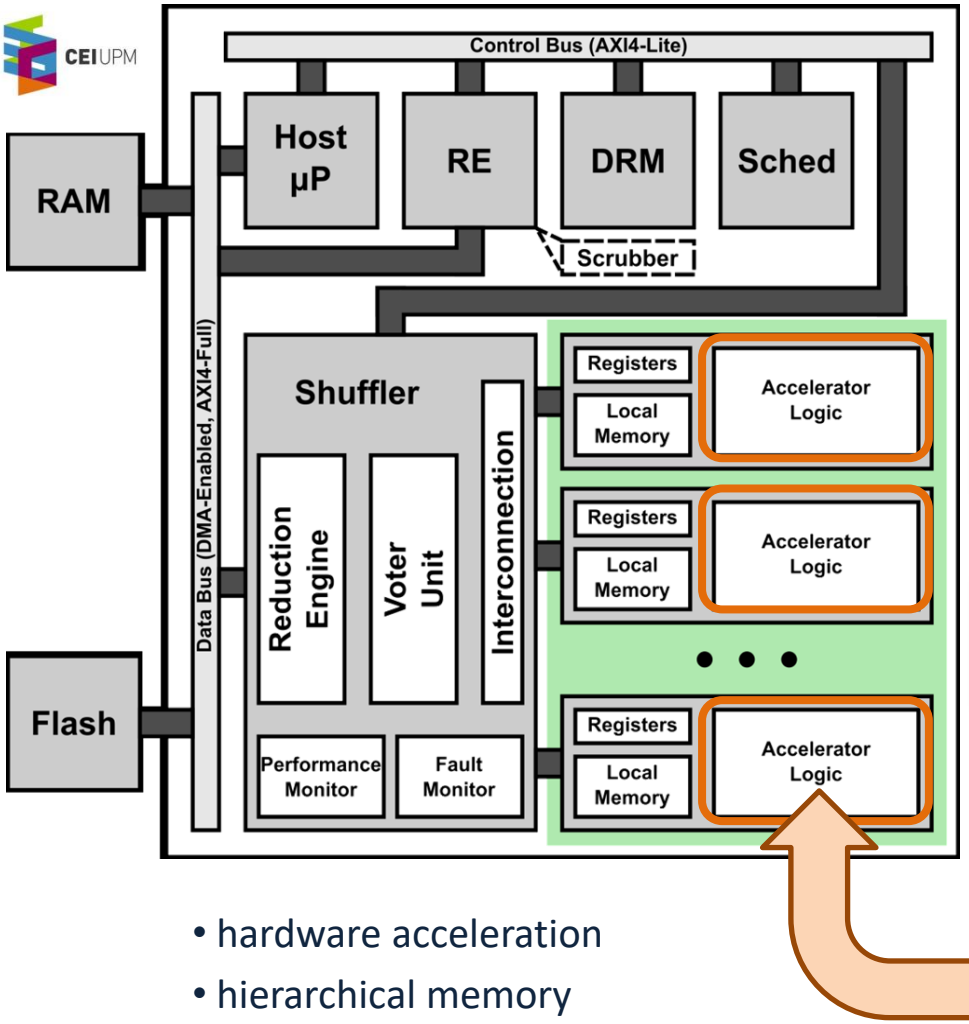
- bus based, DMA enabled communication



Providing Further Degrees of Reconfigurability

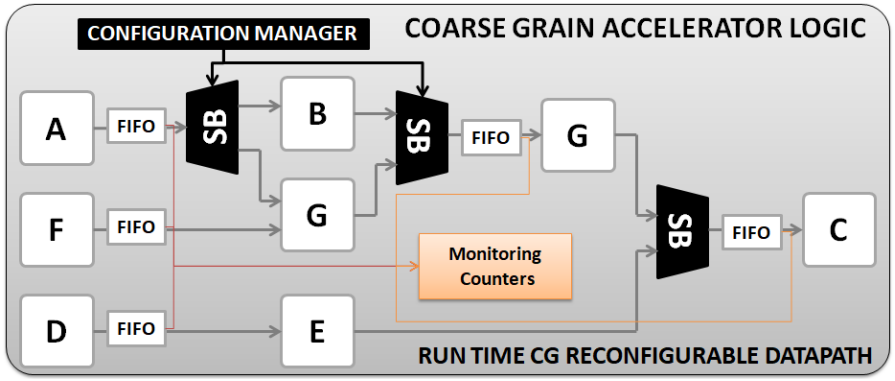
CG into Artico^3



- hardware acceleration
- hierarchical memory
- bus based, DMA enabled communication

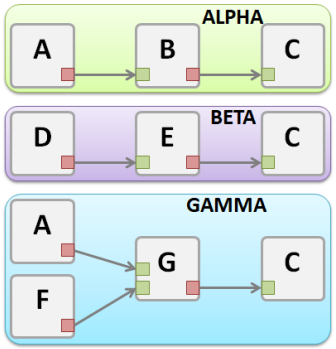
Artico3 is a **DPR** supporting architecture in charge of smartly manage **performance**, **consumption** and **dependability**.

- enhance **flexibility** by enabling CGR within Artico3 slots
- exploit dataflow to **facilitate/ automate programmability**



Providing Further Degrees of Reconfigurability

The big picture within CERBERO



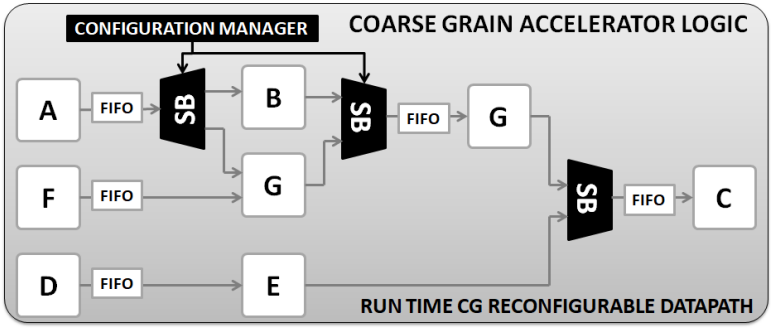
N inputs

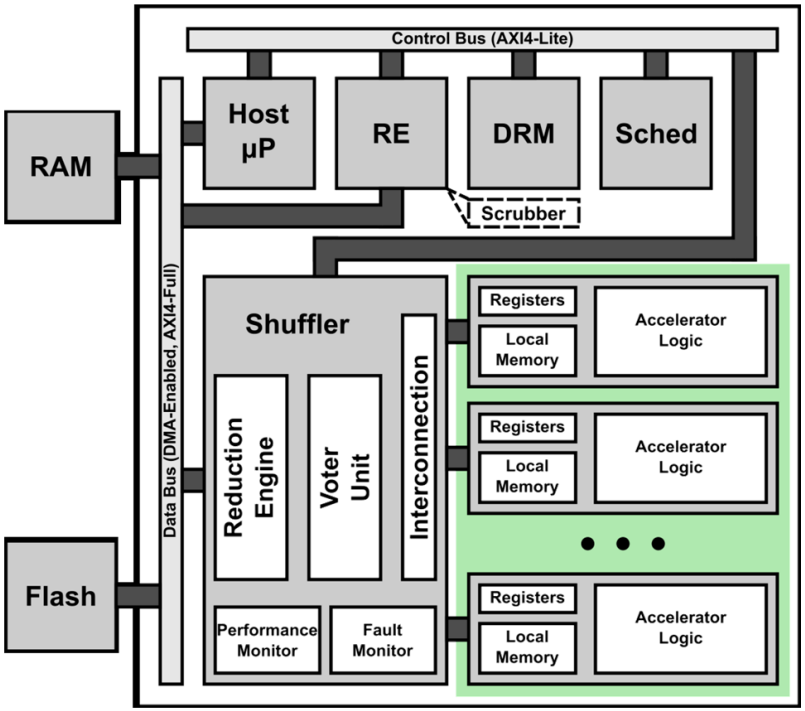
PREESM - N:N

+

MDC - N:1

1 output

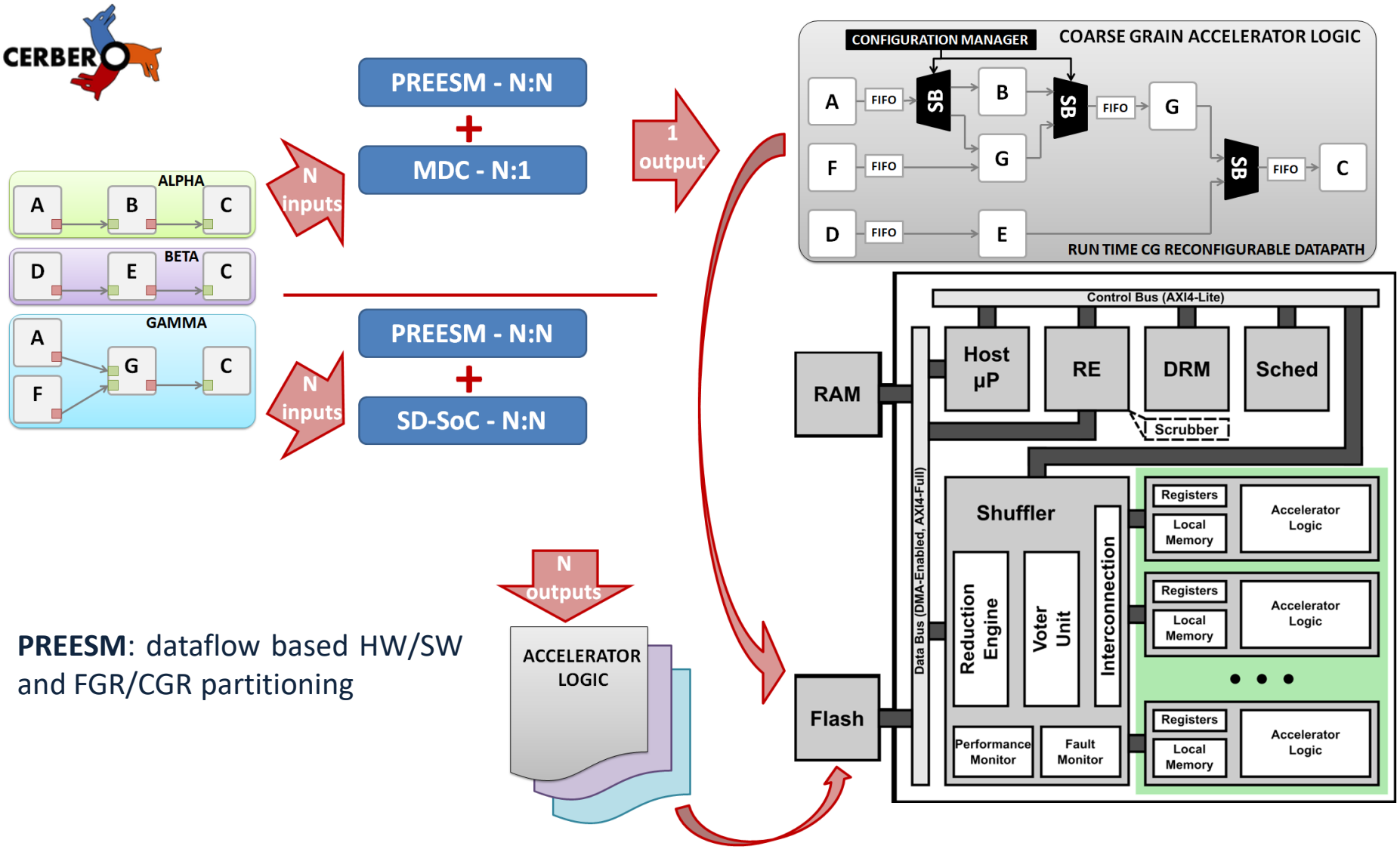




PREESM: dataflow based HW/SW and FGR/CGR partitioning

Providing Further Degrees of Reconfigurability

The big picture within CERBERO



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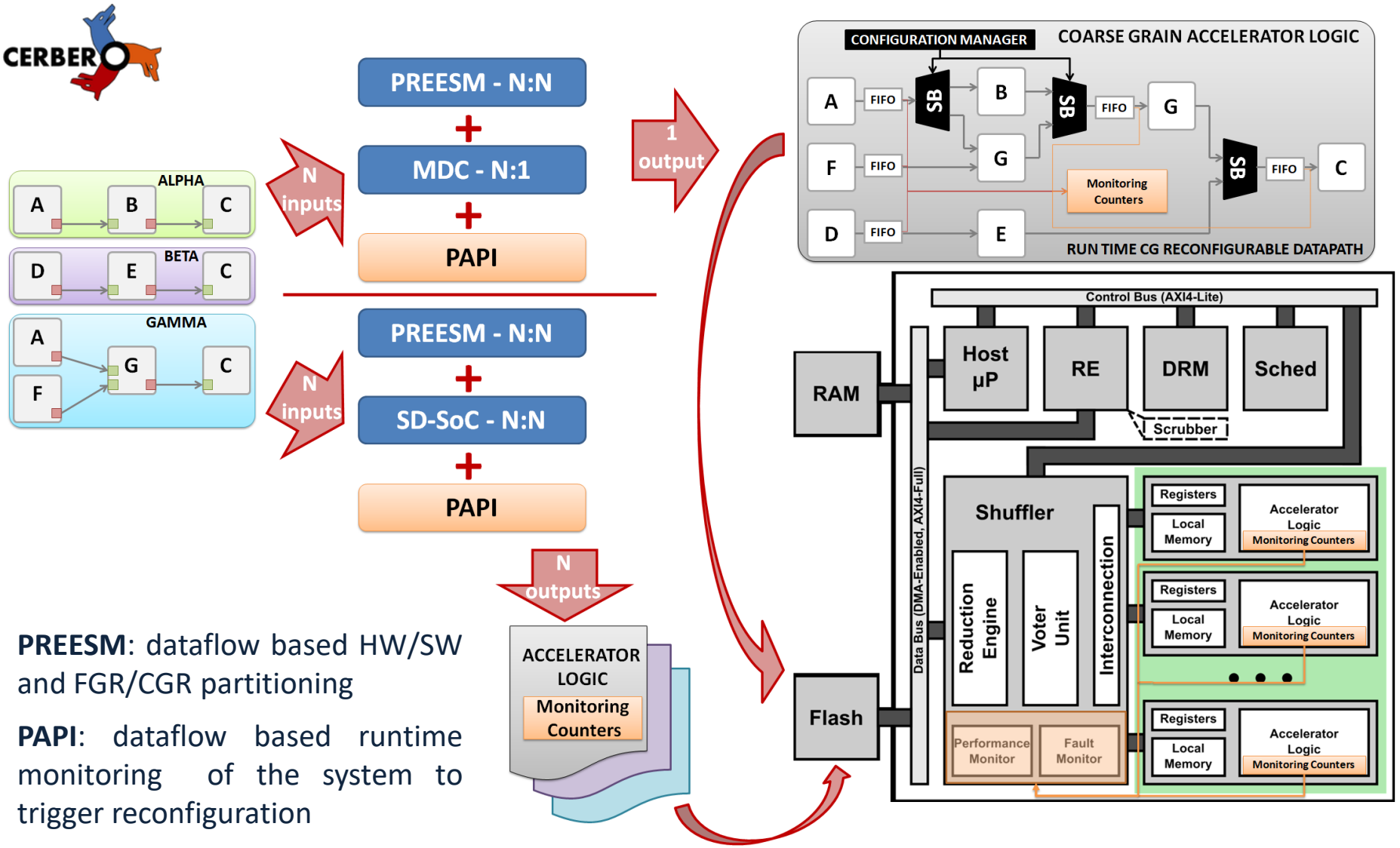
Providing Further Degrees of Reconfigurability

The big picture within CERBERO

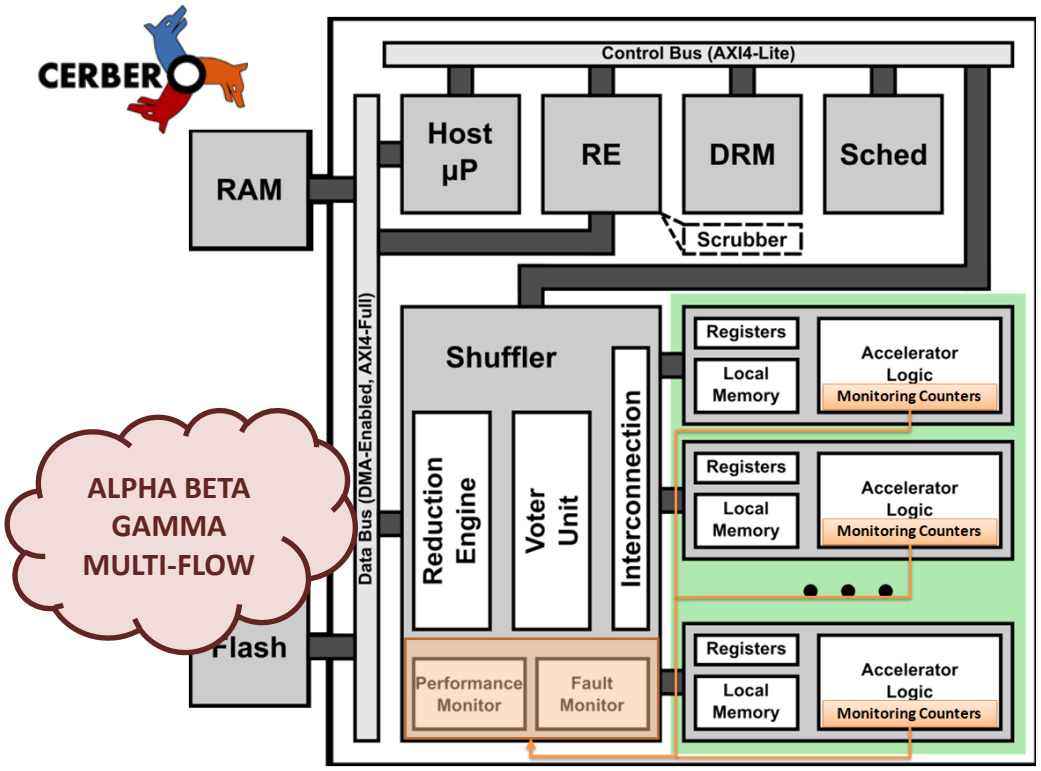


PREESM: dataflow based HW/SW and FGR/CGR partitioning

PAPI: dataflow based runtime monitoring of the system to trigger reconfiguration

Providing Further Degrees of Reconfigurability

The big picture within CERBERO



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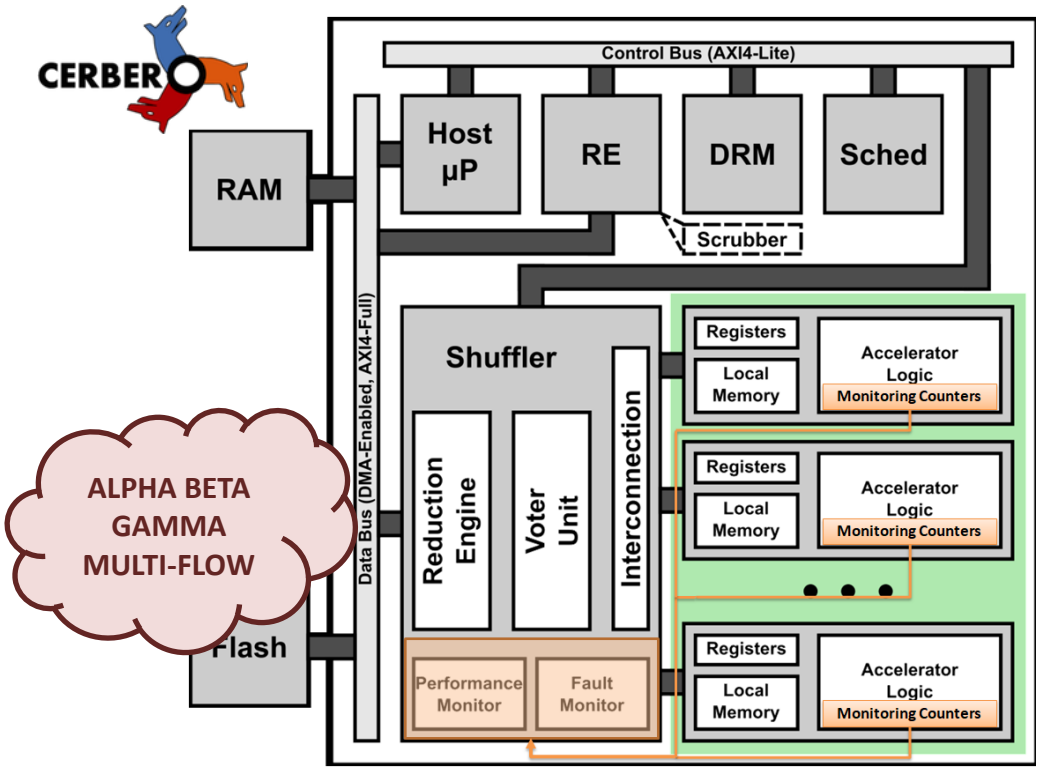
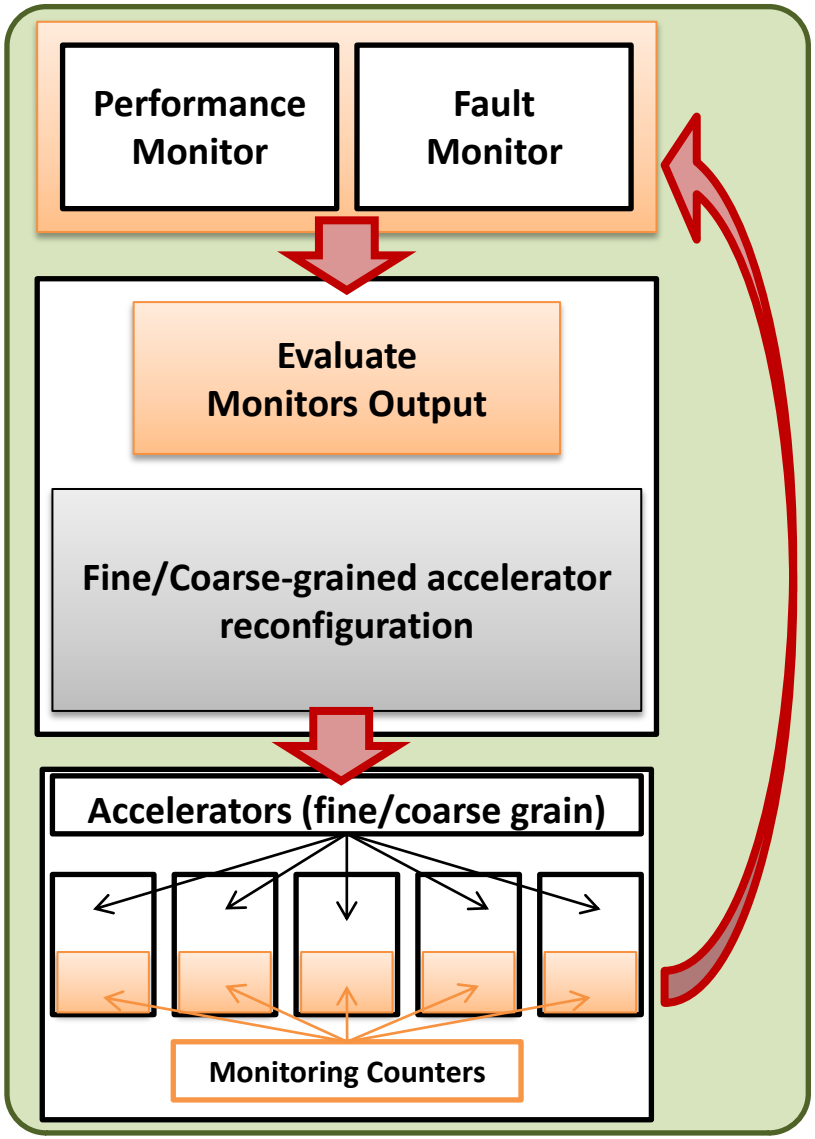
Providing Further Degrees of Reconfigurability

The big picture within CERBERO





PREESM: dataflow based HW/SW and FGR/CGR partitioning

PAPI: dataflow based runtime monitoring of the system to trigger reconfiguration

Thanks To …

EU Commission for funding the ***CERBERO*** (*Cross-layer modEl-based fRamework for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments*) project as part of the H2020 Programme under grant agreement No 732105.

Coordinator:

Michal Masin (IBM), michaelm@il.ibm.com

Scientific Coordinator:

Francesca Palumbo (UniSS), fpalumbo@uniss.it

Innovation Manager:

Katiuscia Zedda (Abinsula), katiuscia.zedda@abinsula.com

Dissemination-Communication Manager:

Francesco Regazzoni (USI), francesco.regazzoni@usi.ch

www.cerbero-h2020.eu

info@cerbero-h2020.eu

@CERBERO_h2020

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Francesca Palumbo, Claudio Rubattu,
Carlo Sau, Tiziana Fanni, Luigi Raffo

INSA

Rennes, 12-14 December 2017