Applications in Electronics Pervading Industry, Environment and Society

ApplePies2017

Challenging CPS Trade-Off Adaptivity with Coarse-Grained Reconfiguration

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21-22 September 2017 – Rome (IT)

Outline

- Introduction
  - *Cyber Physical Systems*
  - *Coarse-Grained Reconfiguration*
  - *Multi-Dataflow Composer tool*
- Dynamic Trade-off Management
  - *Manually implemented CGR AES on FPGA*
  - *Automatically Derived HEVC interpolator on FPGA*
  - *Automatically Derived and Optimized FFT on ASIC*
- Experimental Results
- Conclusions

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Complex systems with **different interacting and deeply intertwined components**, providing multiple and distinct **behavioral modalities** potentially **changing over time**, that contribute **concurrently** to determine the behavior of the system as a whole.

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Subjected to **Functional** (F) and **Non-Functional** (NF) requirements variation in time.

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http://www.cerbero-h2020.eu/

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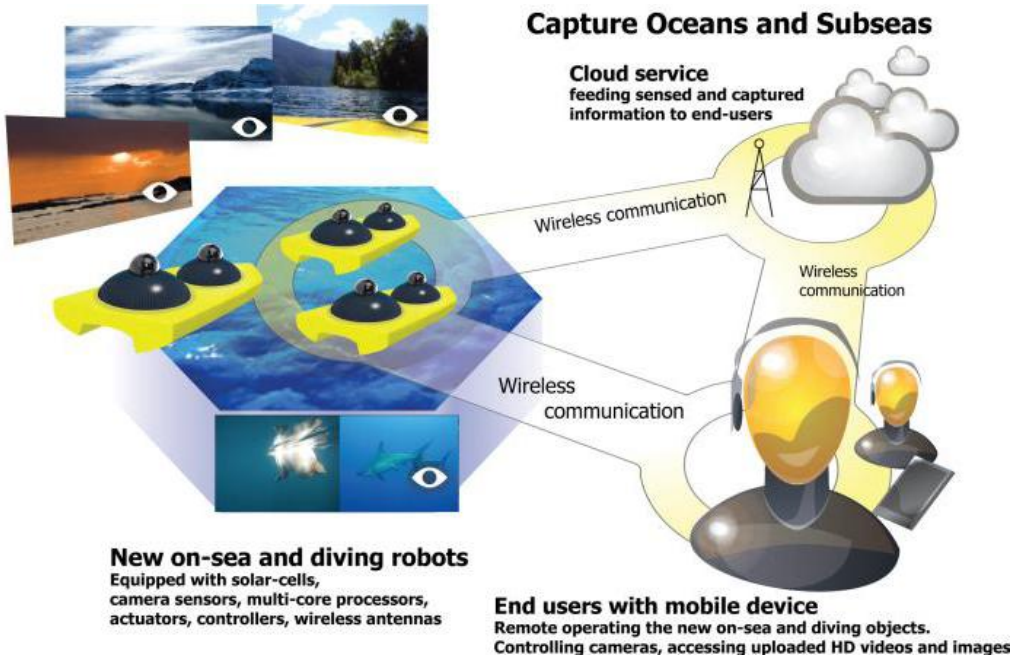

Coarse-Grained Reconfigurable(CGR) Systems

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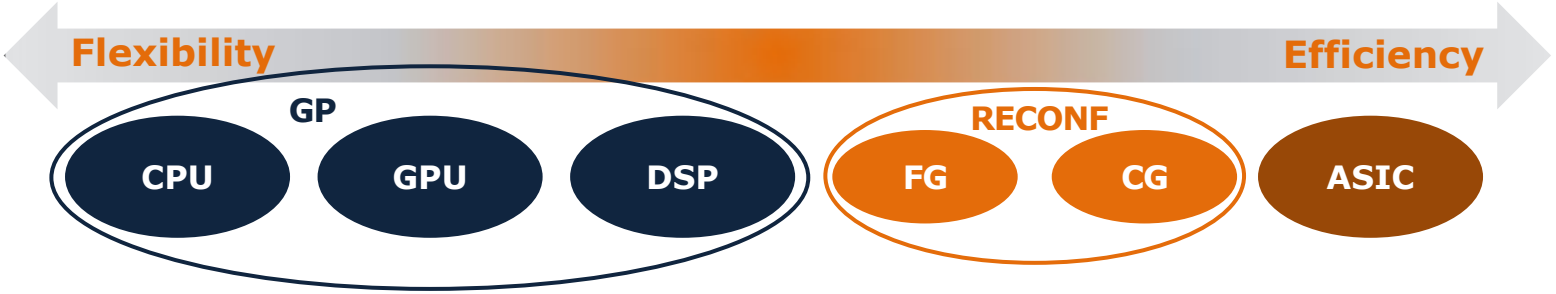

Reconfigurable computing provides a **trade-off between execution efficiency** typical of ASICs **and flexibility** mainly exhibited by GP devices.

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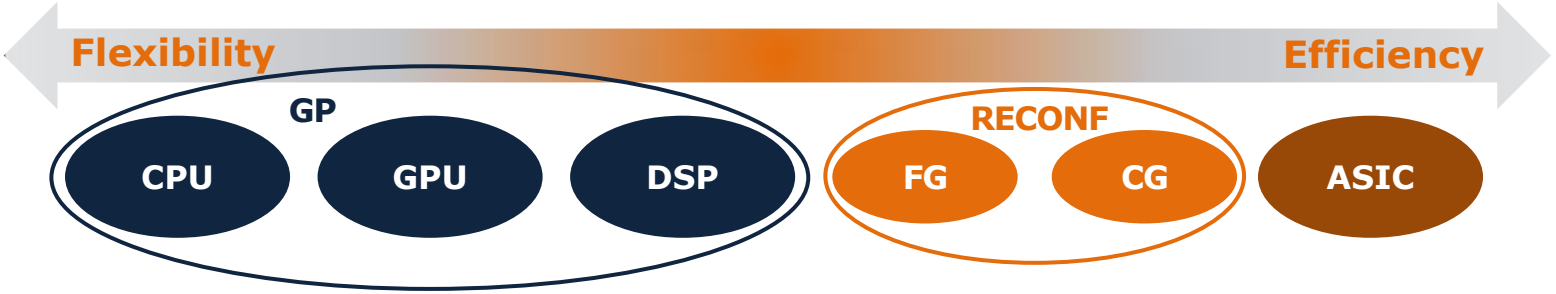

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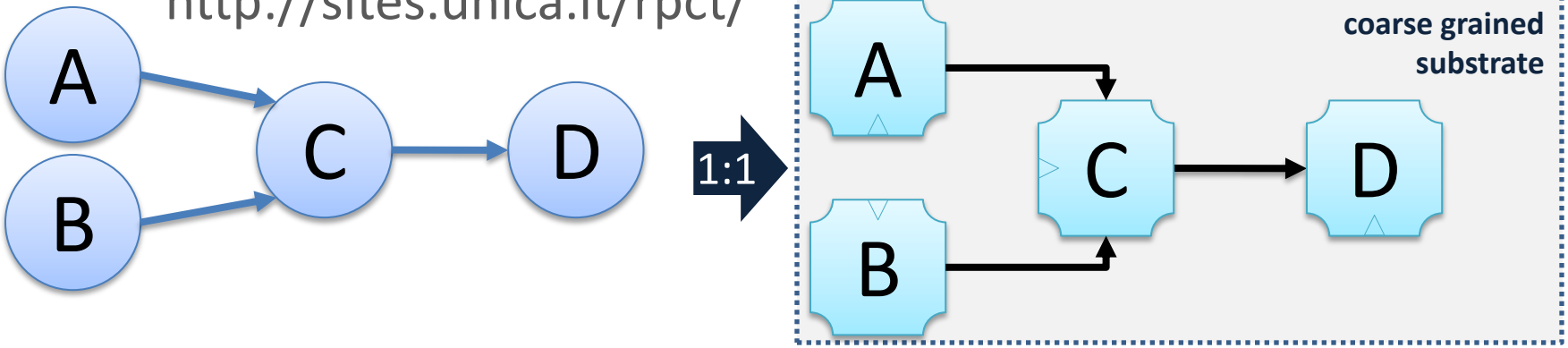
	Fine-Grained (FG) bit-level	Coarse-Grained (CG) word-level
flexibility	☺	😐
speed	😐	☺
memory	☹	😐

Mapping CGR Platforms
Multi-Dataflow Composer (MDC) tool

http://sites.unica.it/rpct/



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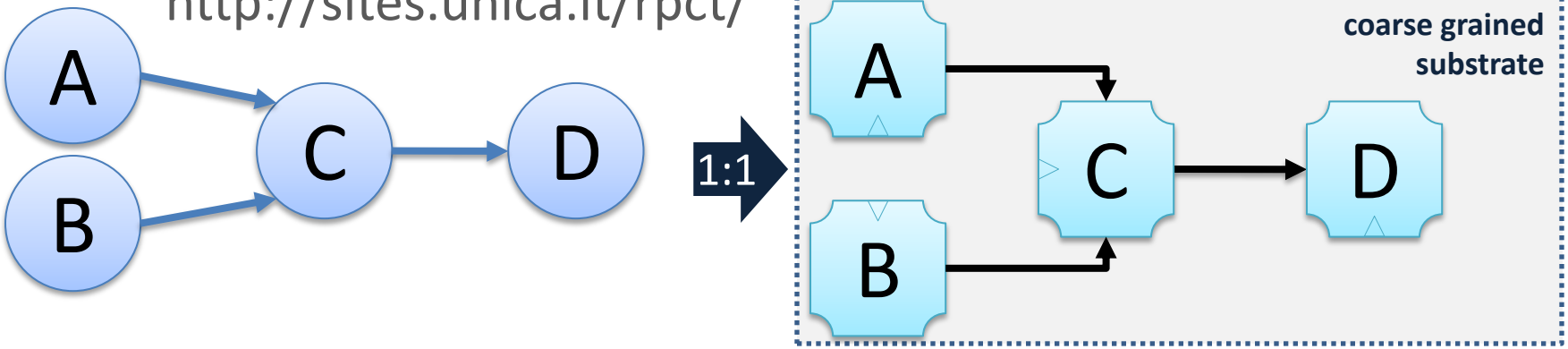

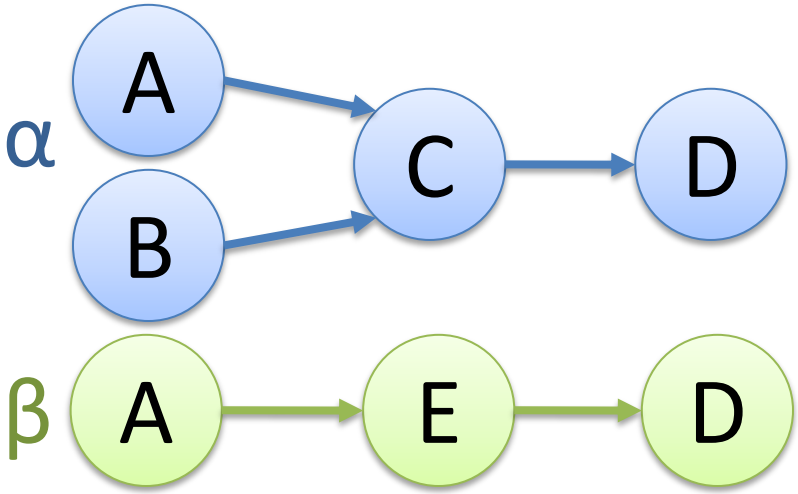

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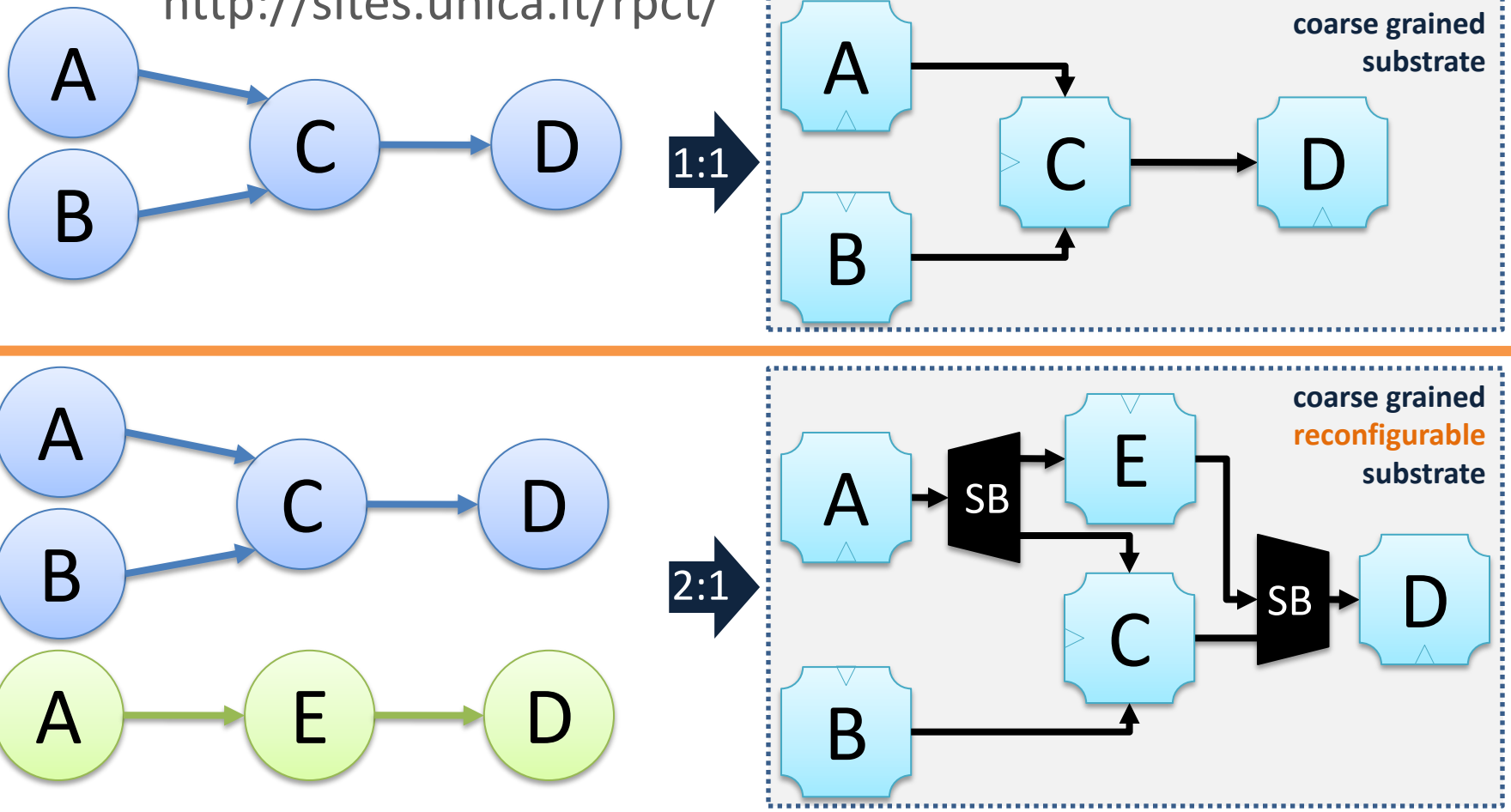

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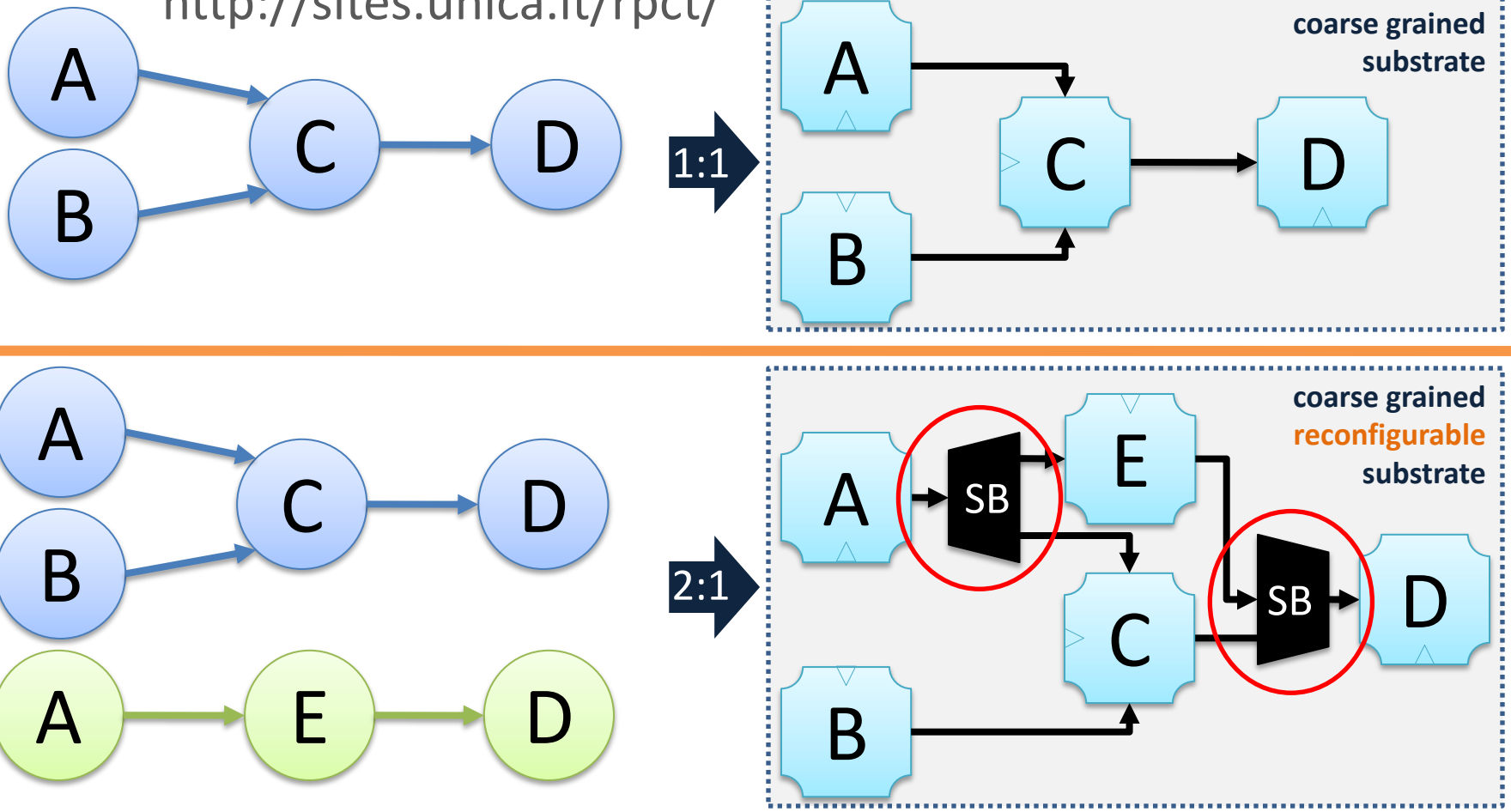

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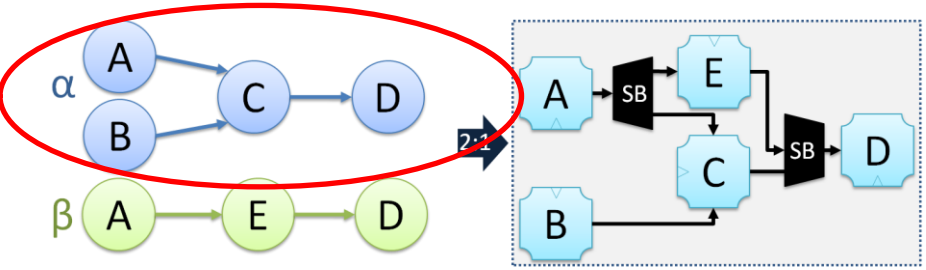

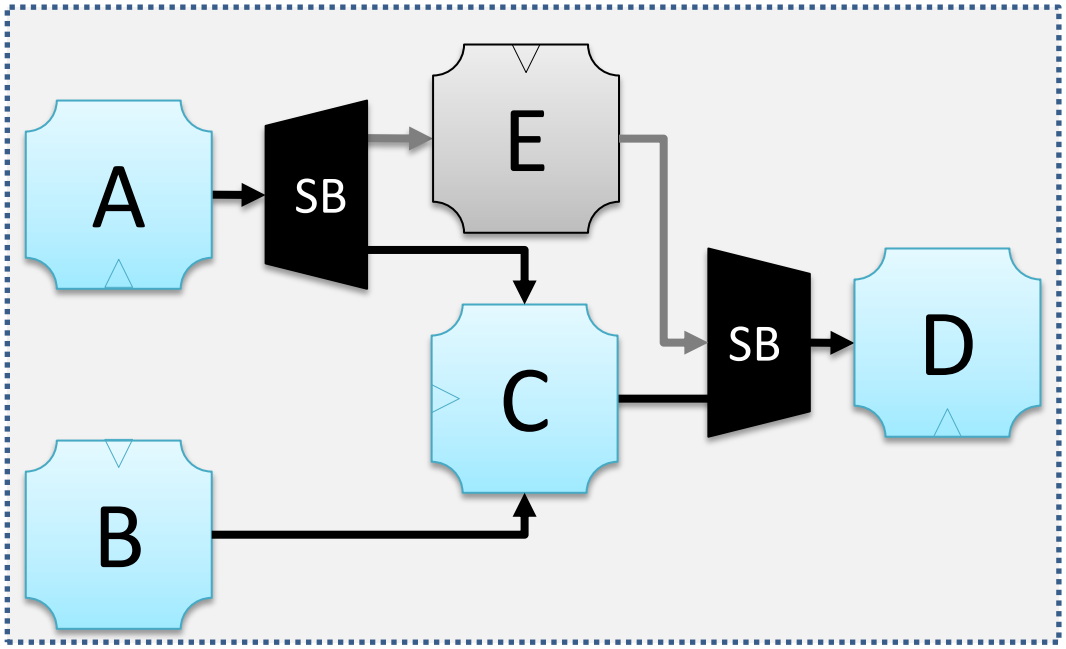

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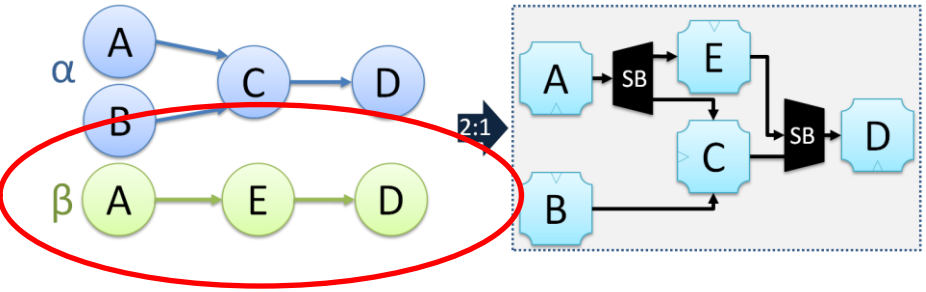

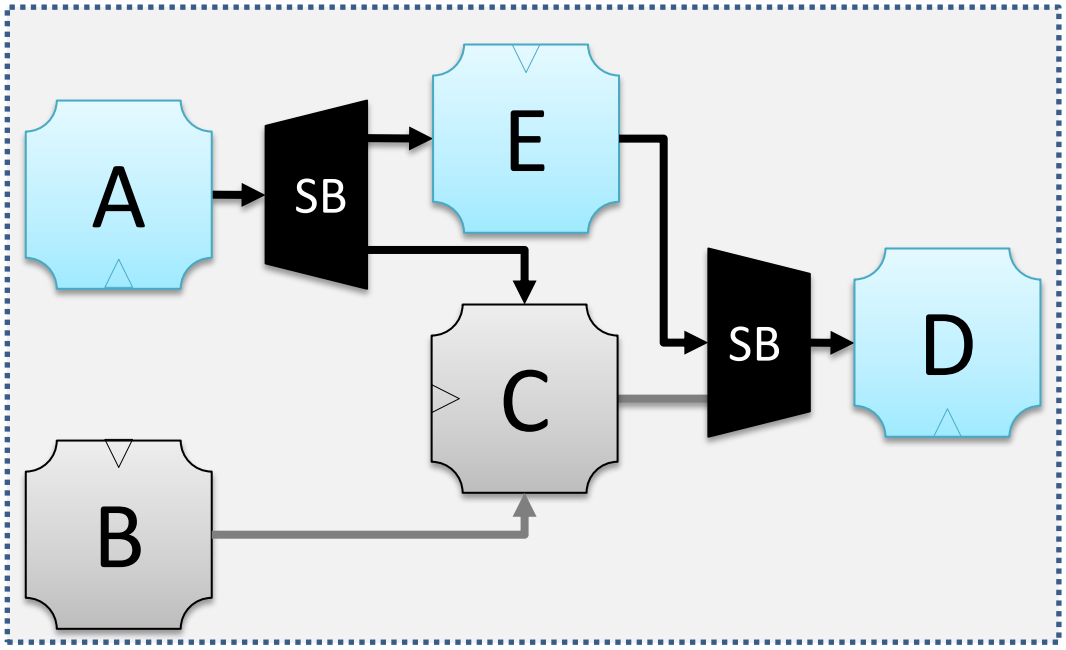

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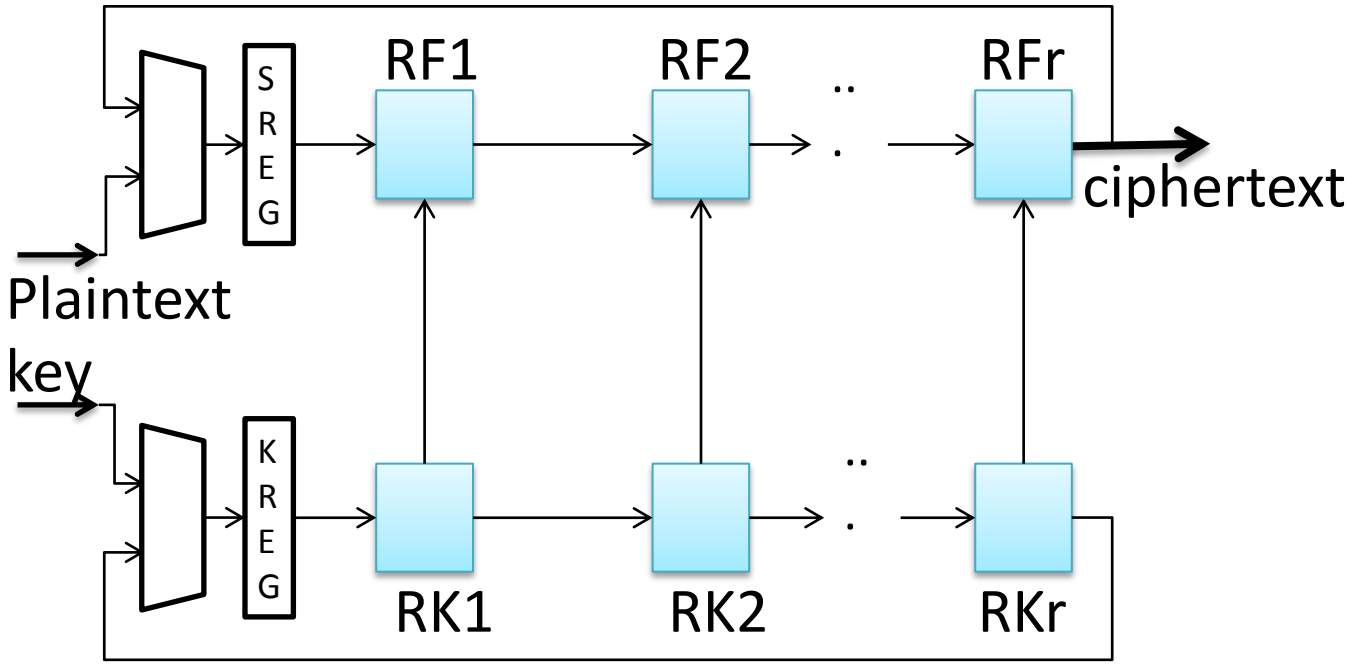
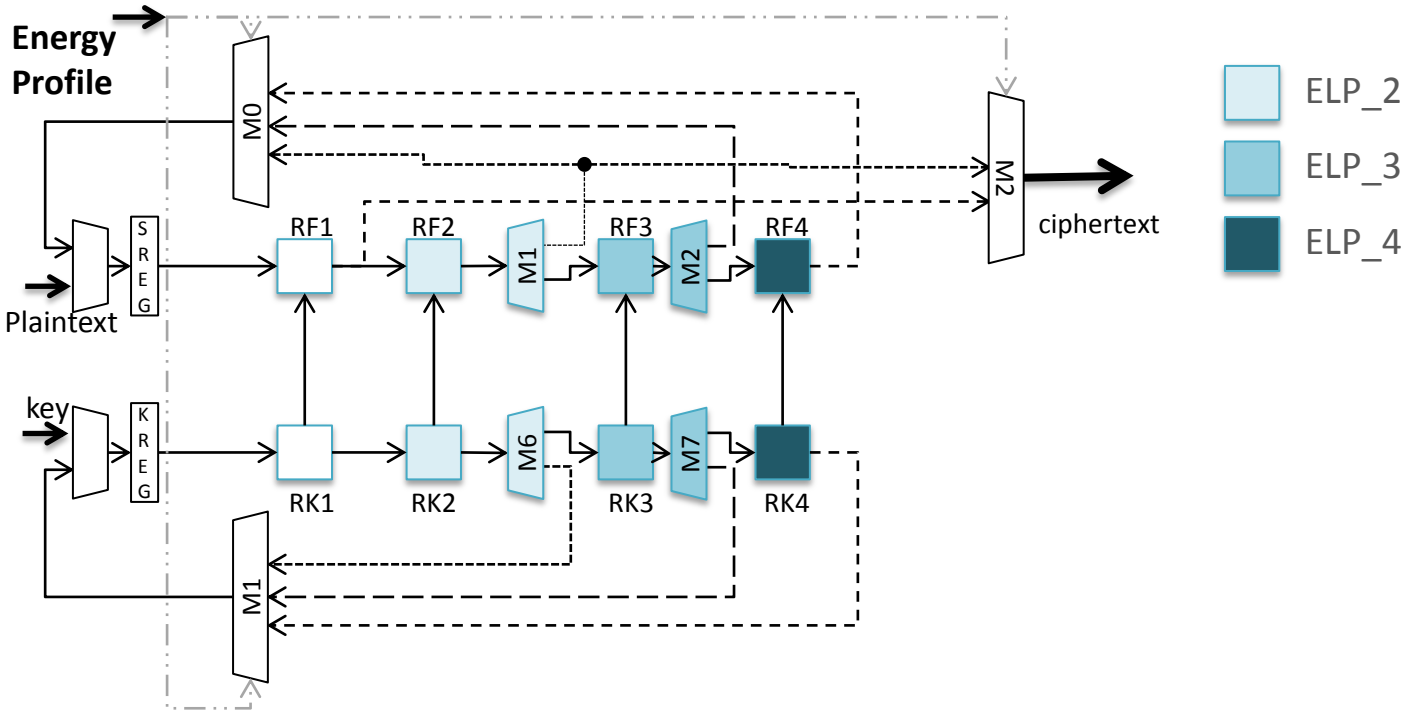
Dynamic Trade-off Management
Advanced Encryption Standard



Selected by the Institute of Standards and Technology to be the standard block cipher.
Several implementations are possible.

Dynamic Trade-off Management
Multi-Profiles AES Implementation



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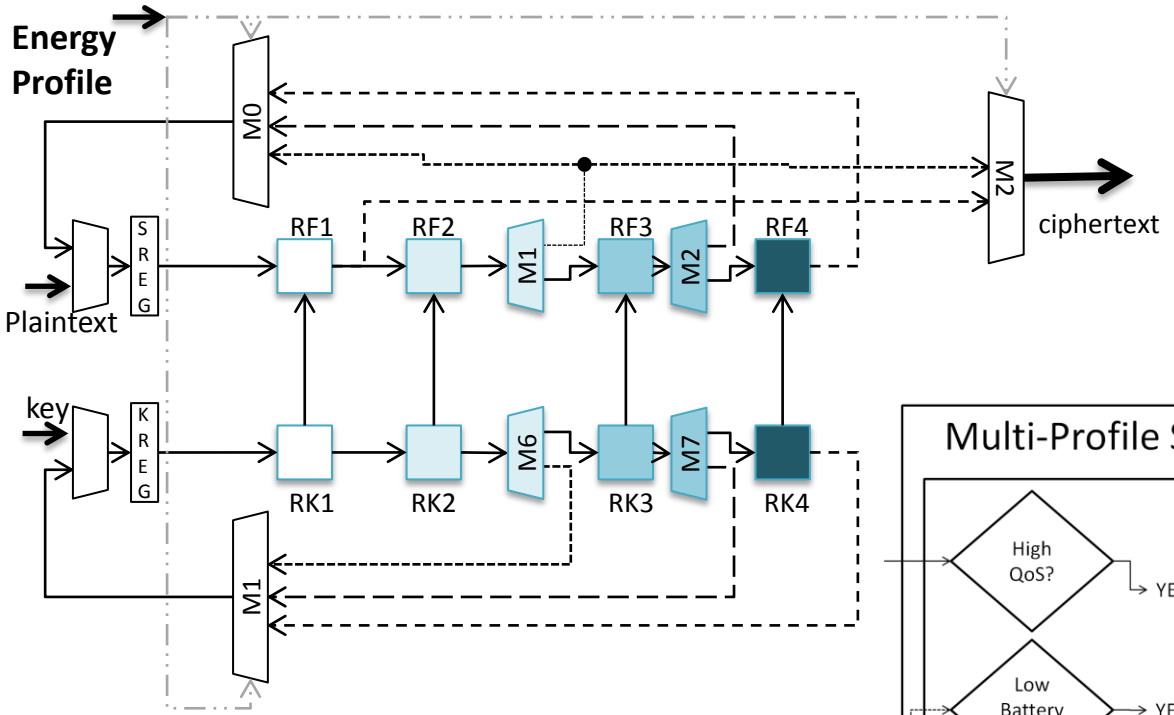

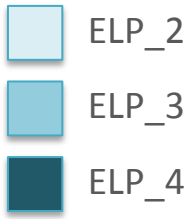

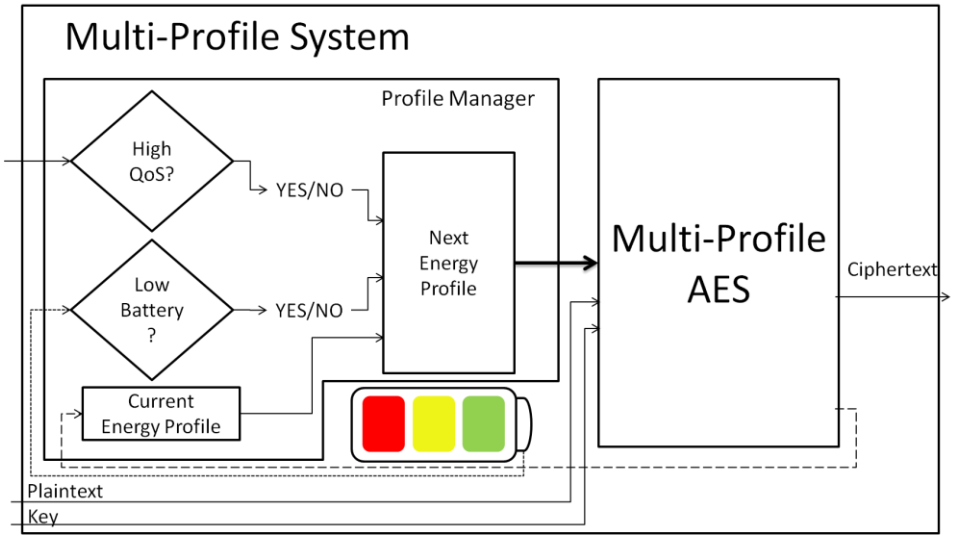

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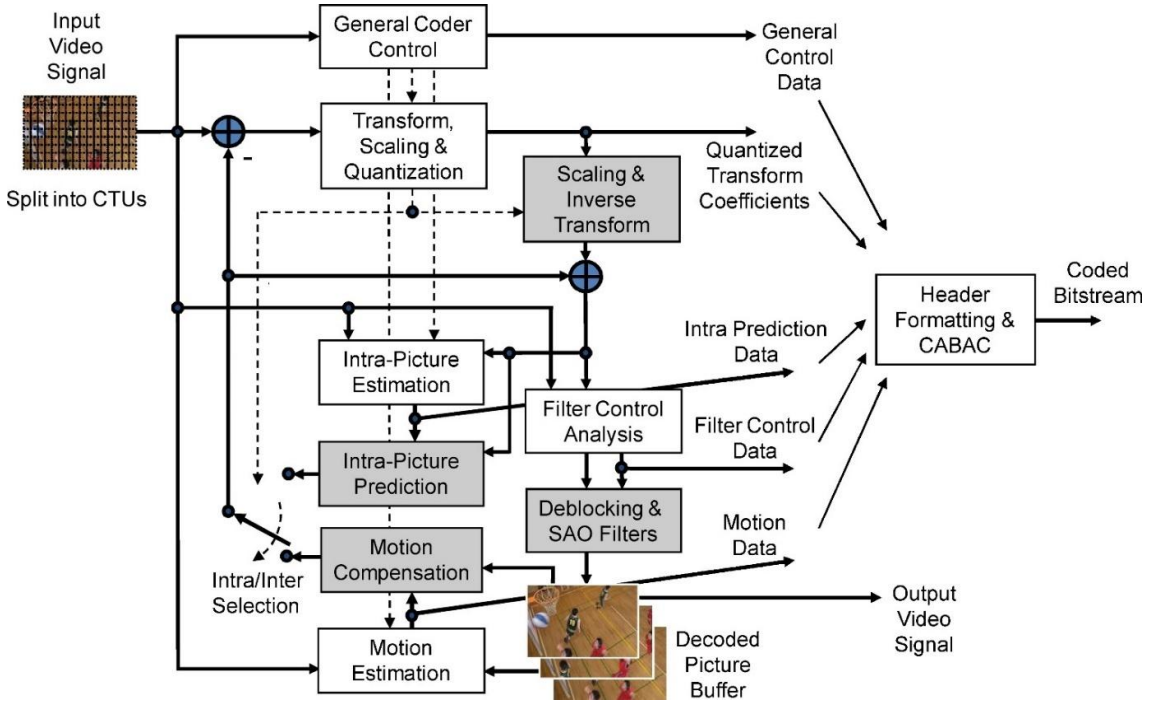
Dynamic Trade-off Management
High Efficiency Video Coding (HEVC)

Recent video codec developed by the Joint Collaboration Team on Video Coding (VCEG and MPEG). It provides up to **50% bit rate reduction at the same subjective video quality** with respect to previous standards (H.264).



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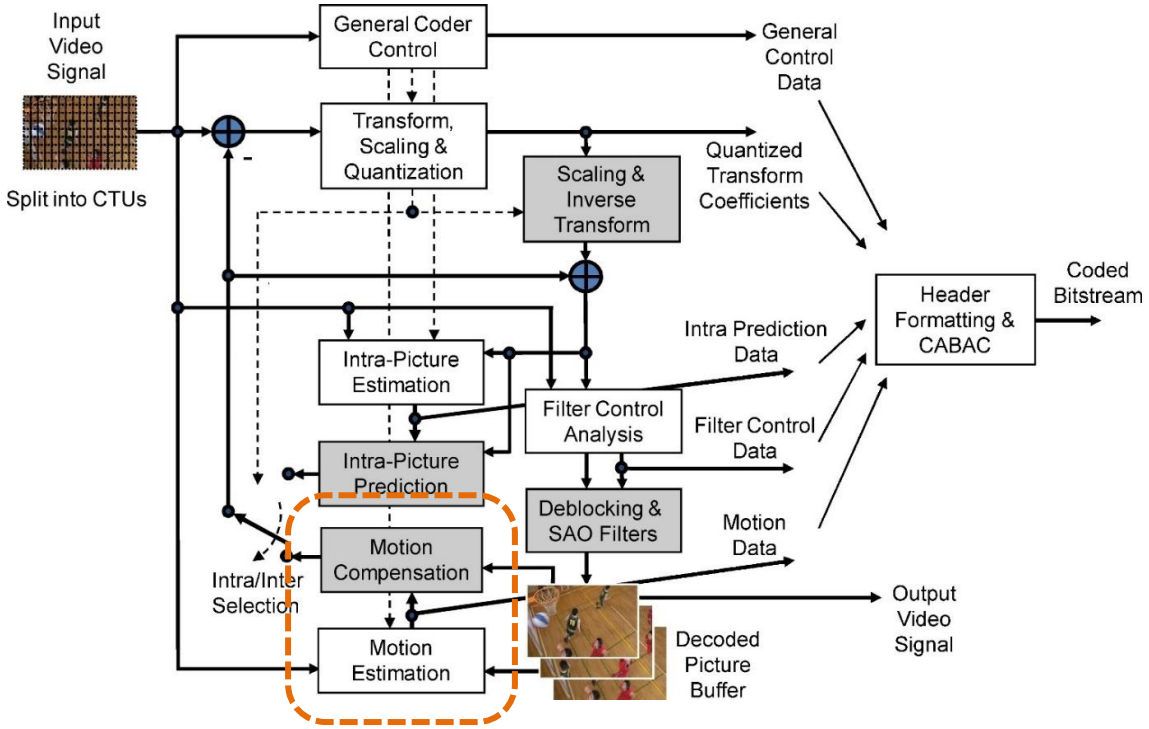

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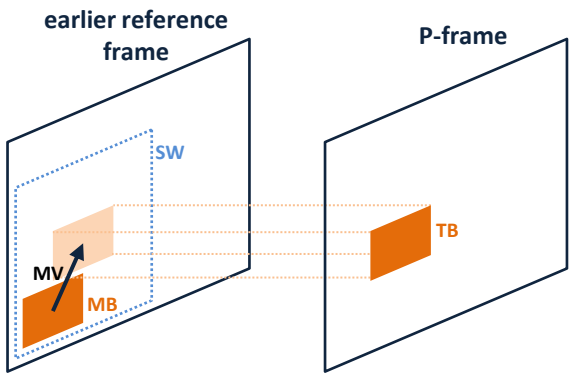
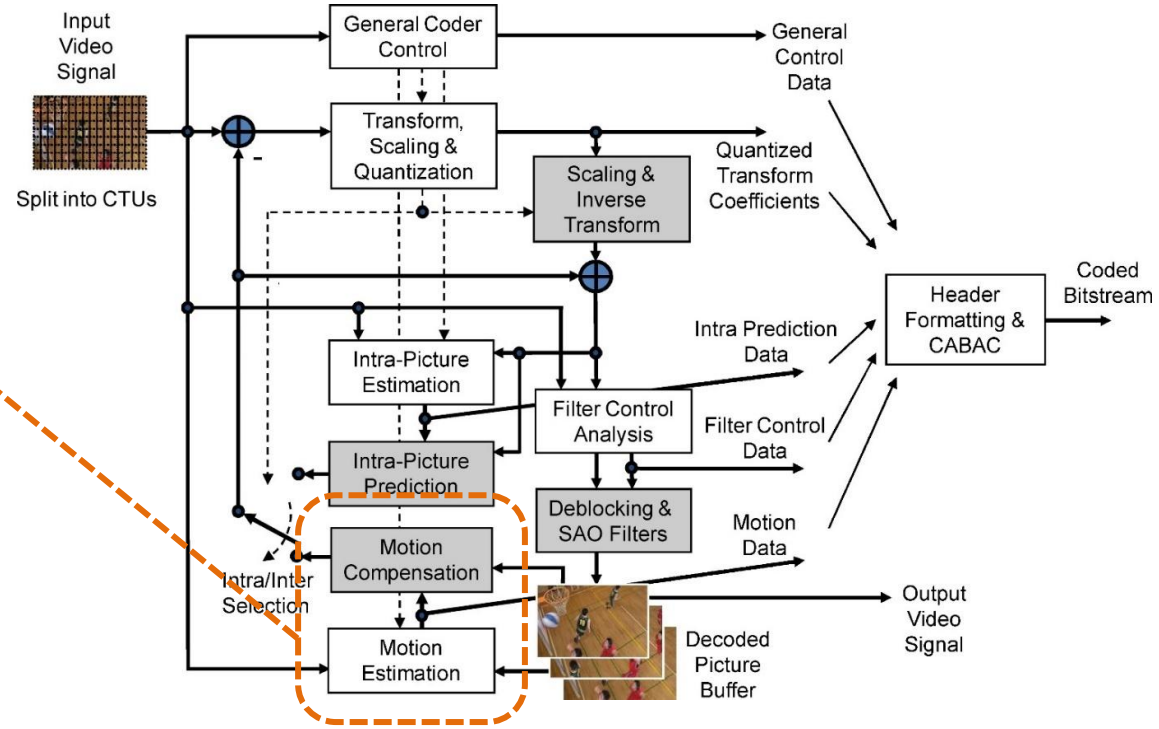
Computational Intensive and Power Hungry Step: Motion Estimation and Compensation





Dynamic Trade-off Management

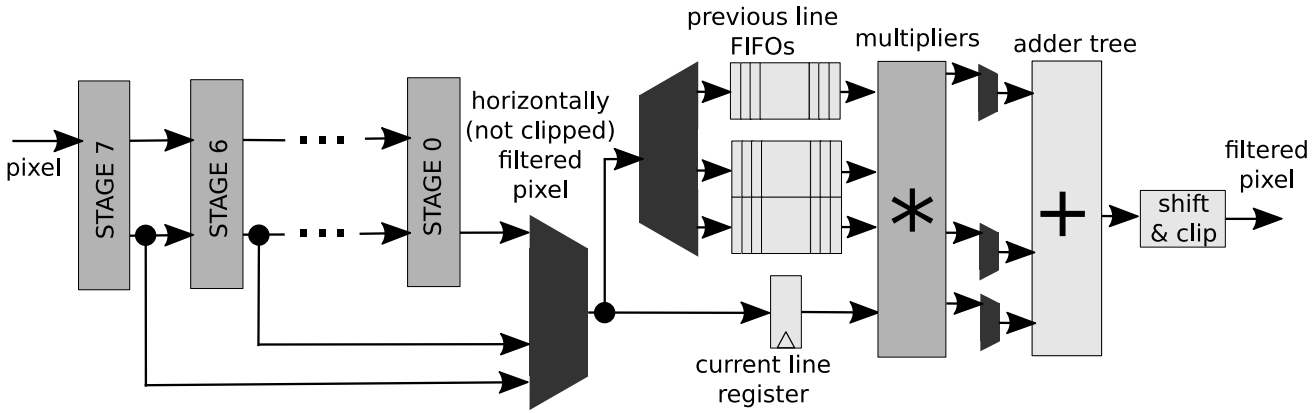
High Efficiency Video Coding (HEVC)

Functional Approximate computing:

Reduce the number of taps in the filters

to save up to 28% of energy

Dynamic Trade-off Management
CGR HEVC Interpolators



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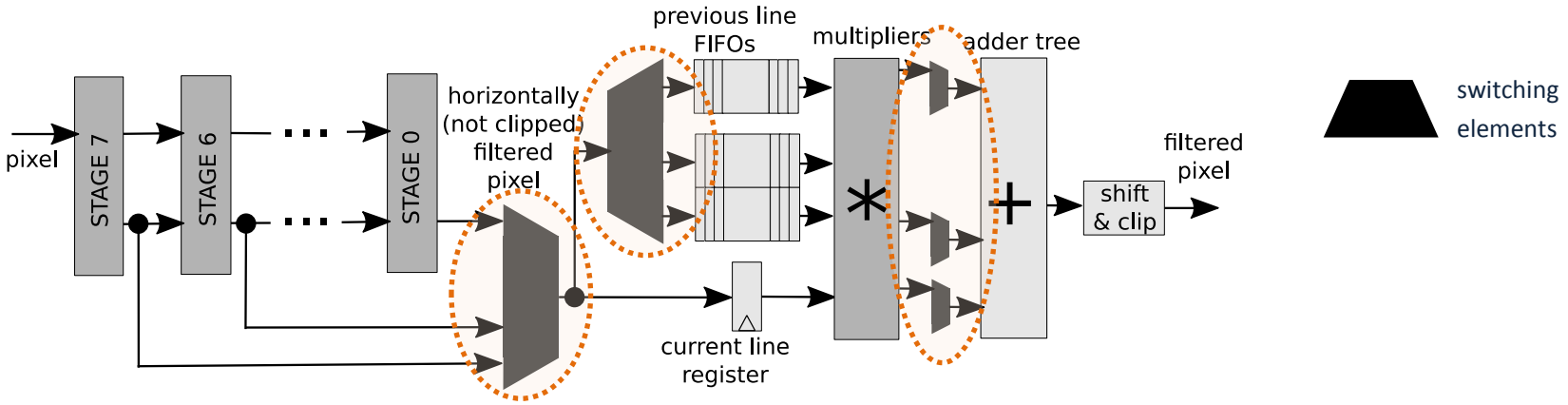

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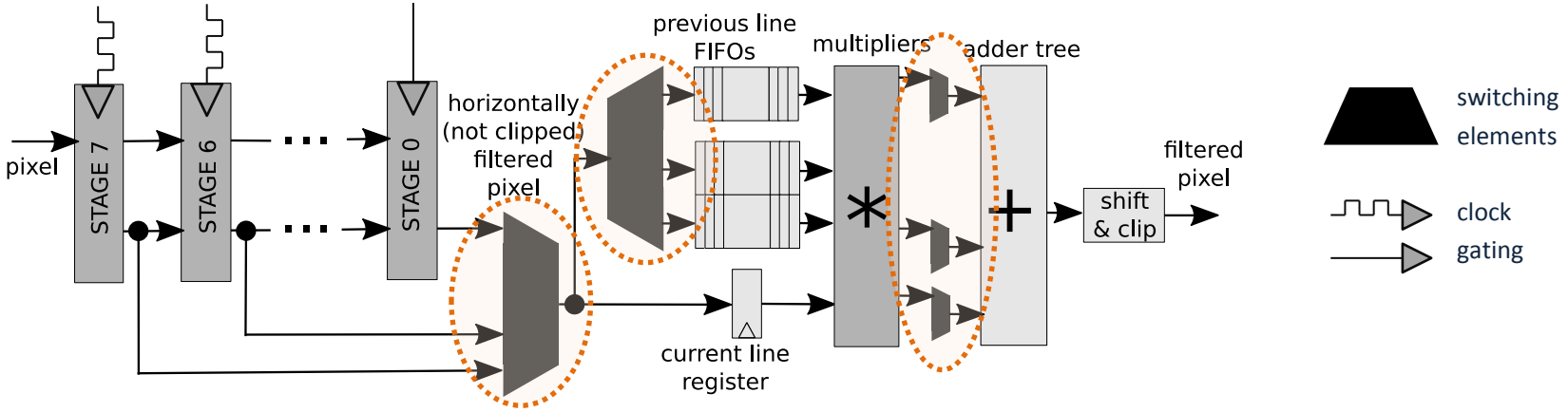

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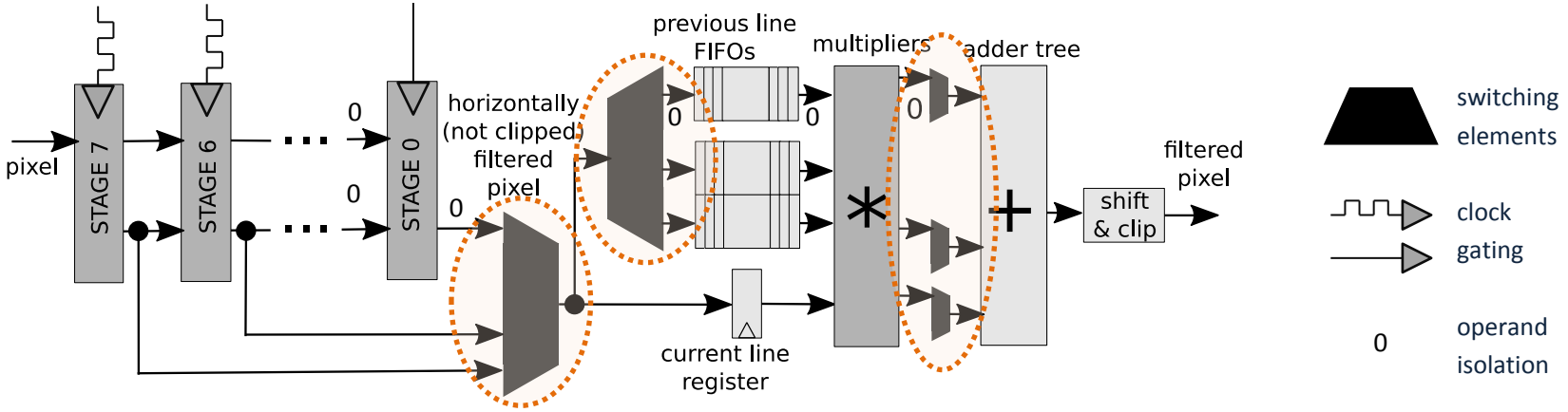

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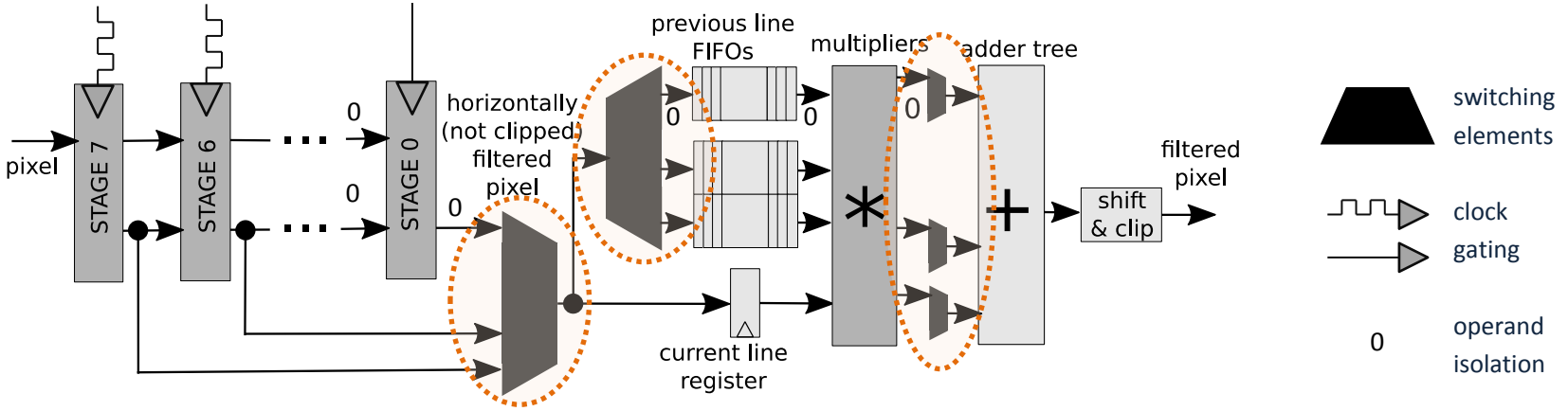

profile	HIGH			MEDIUM			LOW		
	quality	# taps	energy	quality	# taps	energy	quality	# taps	energy
luma	☺	8/7	☹	😐	5	😐	☹	3	☺
chroma		4			3			2	

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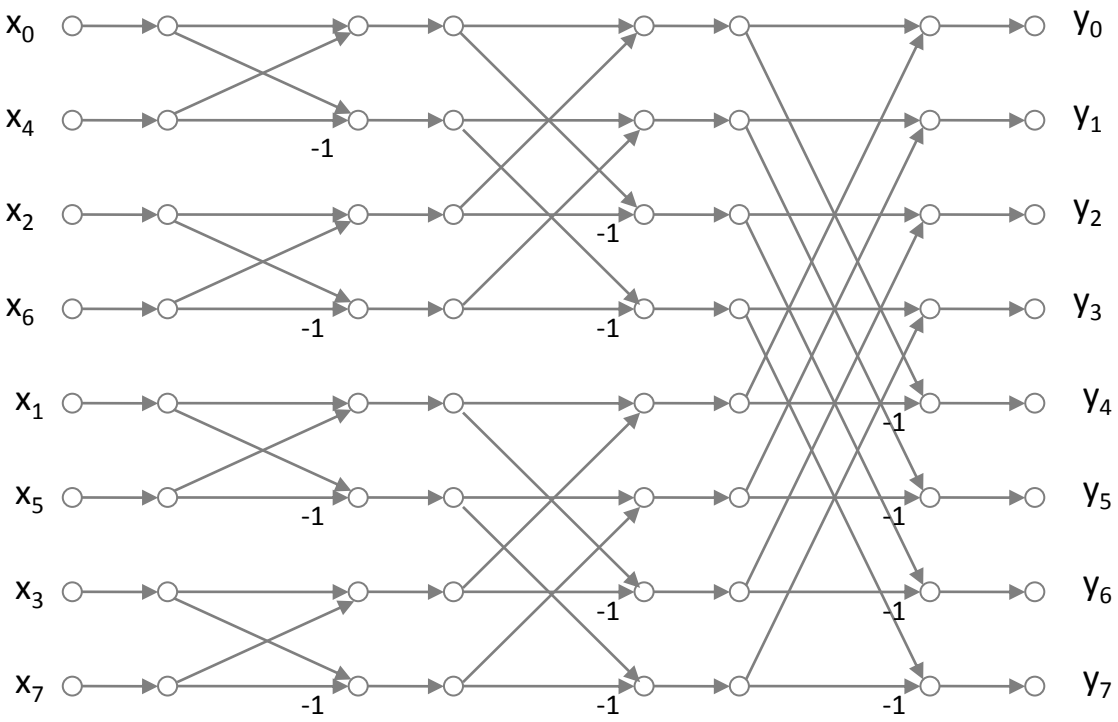
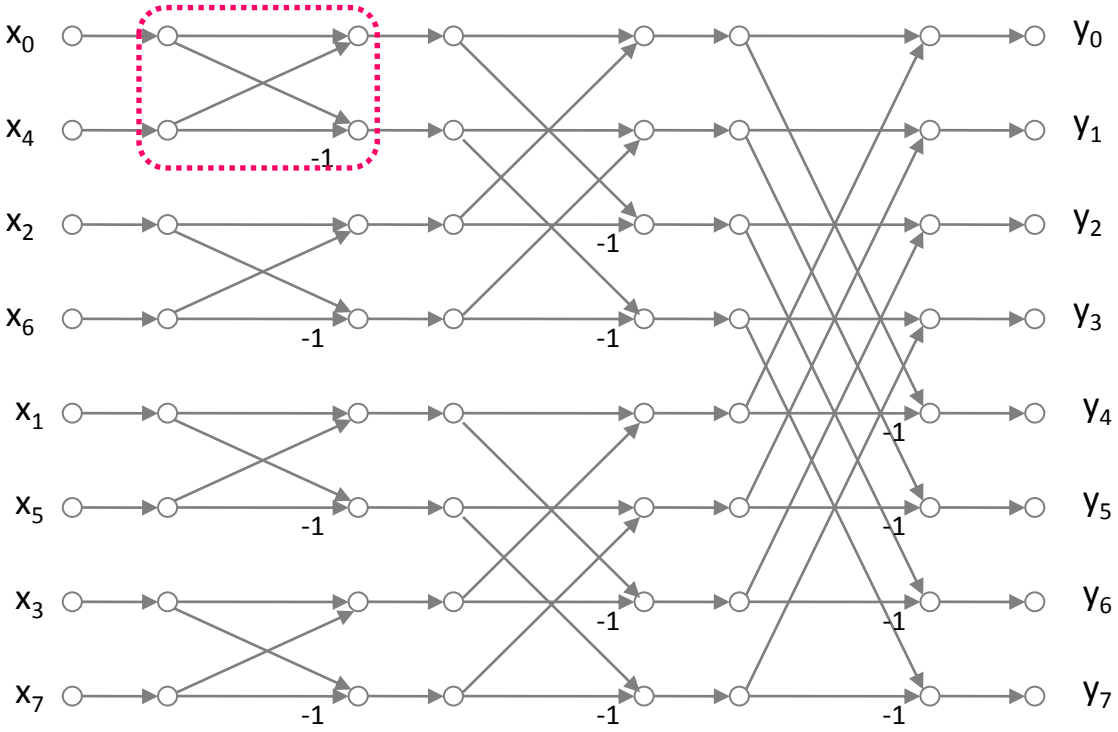
Dynamic Trade-off Management

Fast Fourier Transform (FFT)



Dynamic Trade-off Management
Fast Fourier Transform (FFT)

radix-2 butterfly



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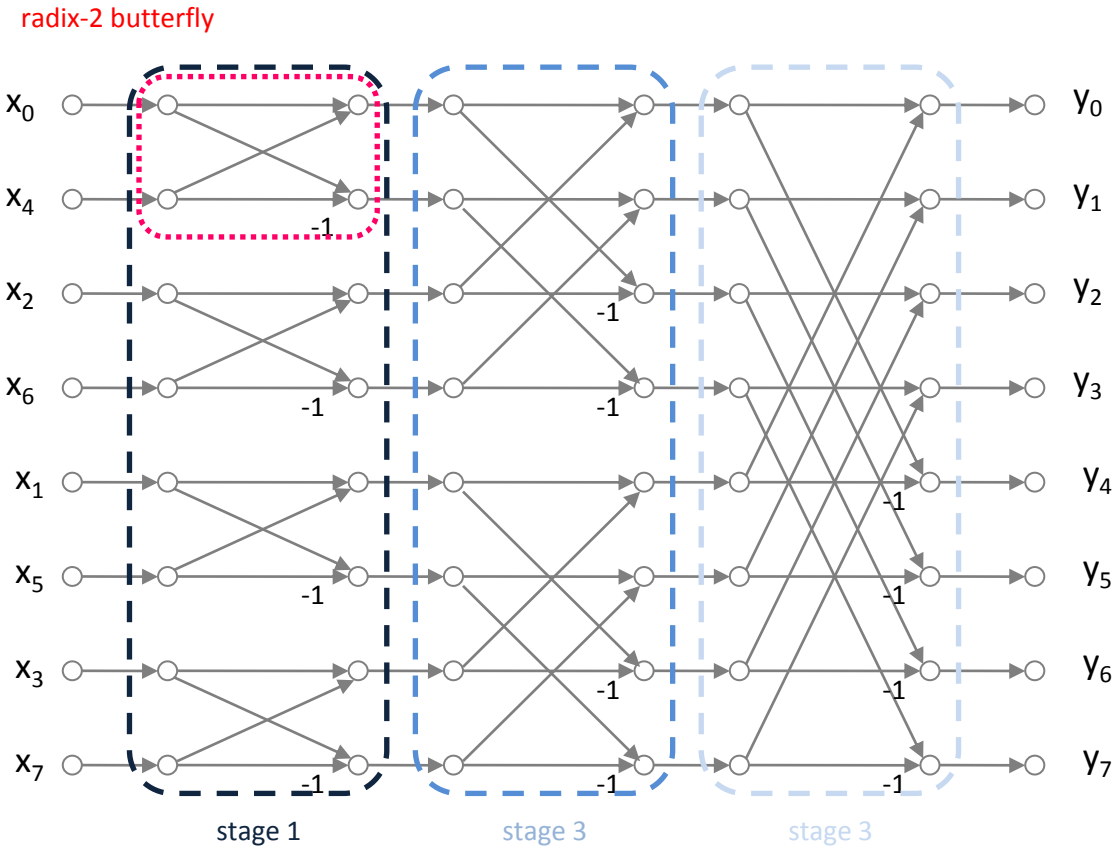

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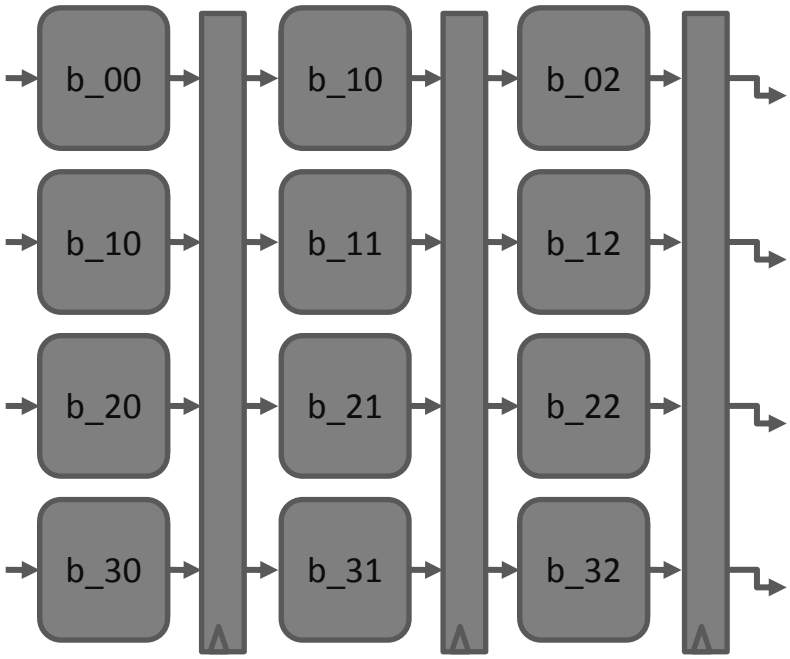

12 butterflies

Dynamic Trade-off Management

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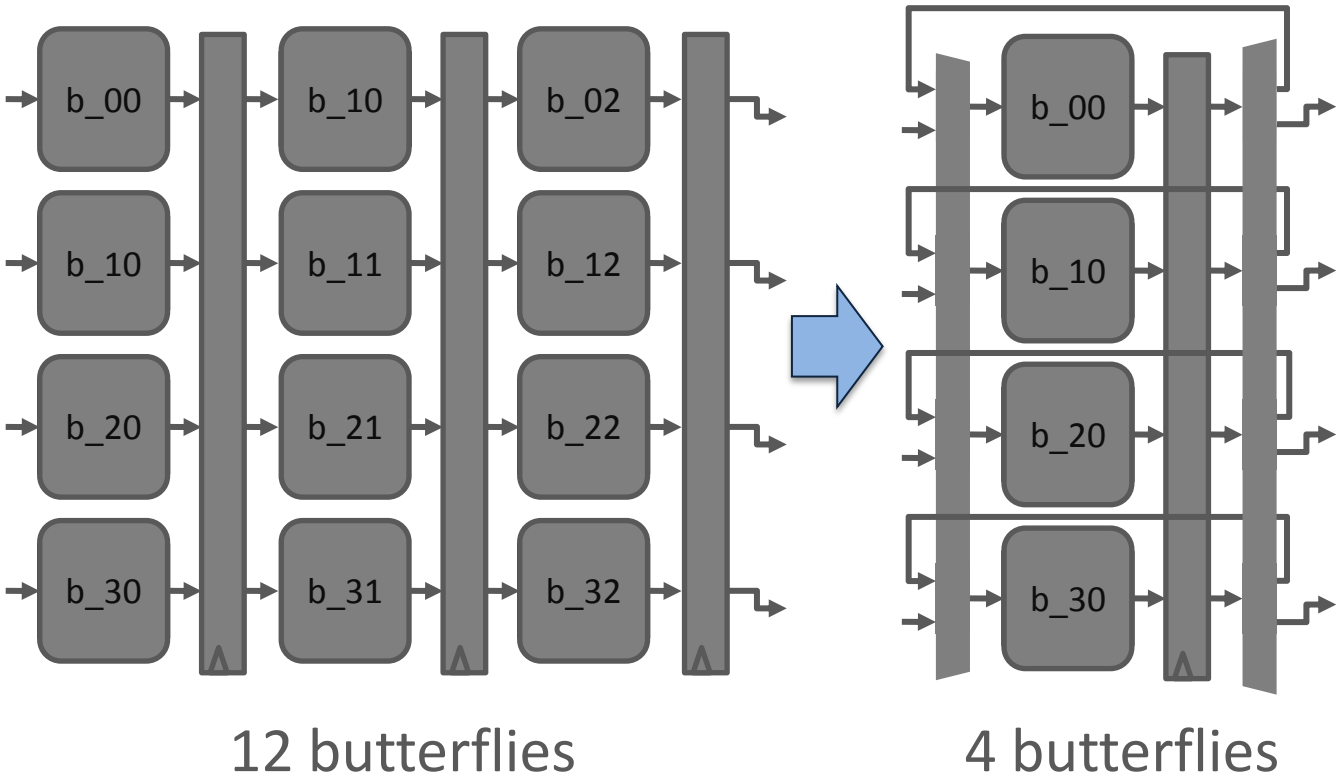

12 butterflies

4 butterflies

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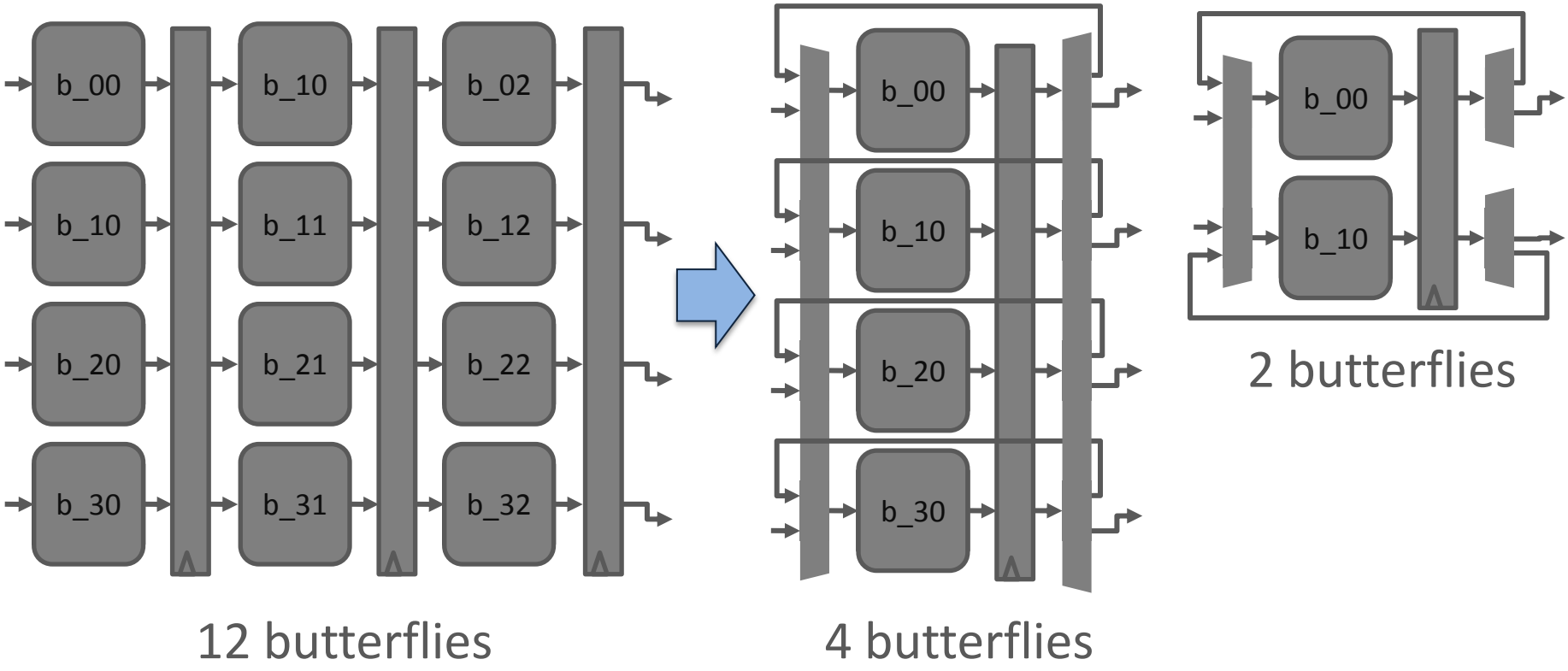

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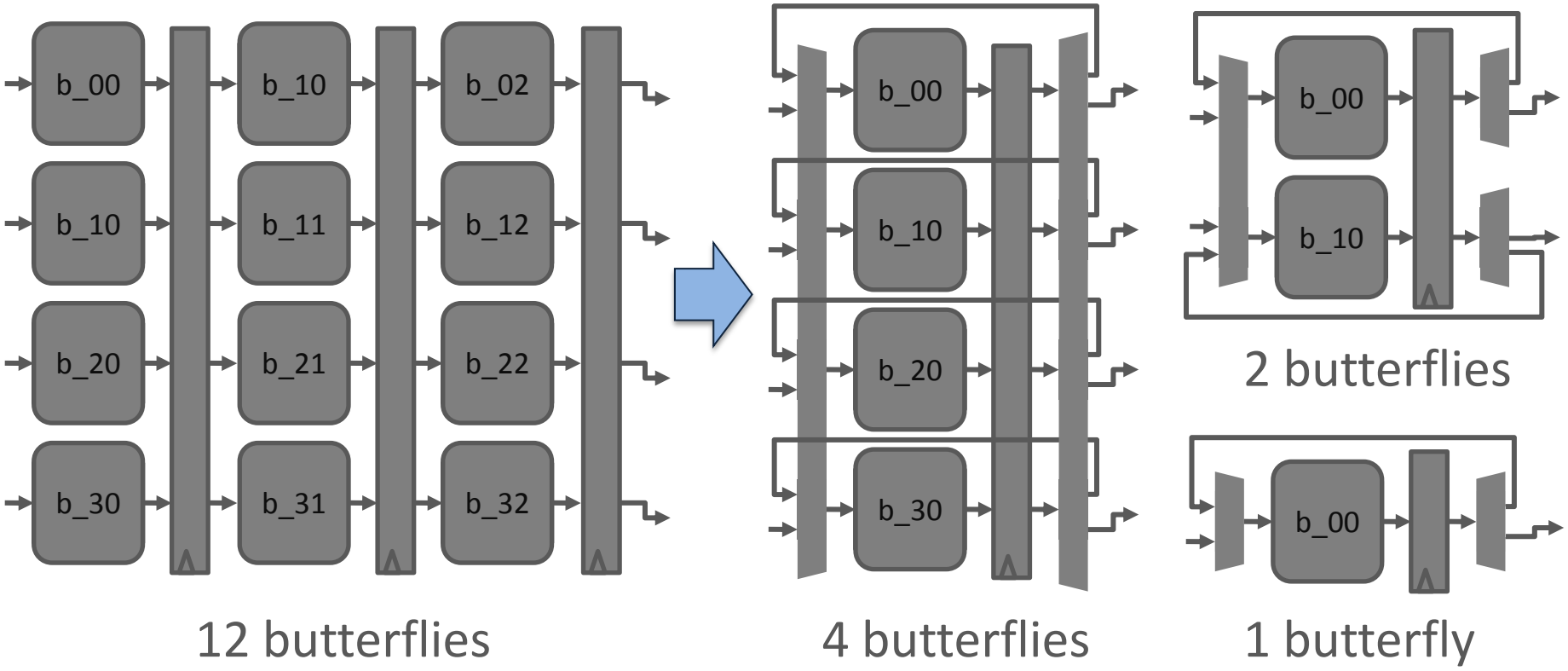
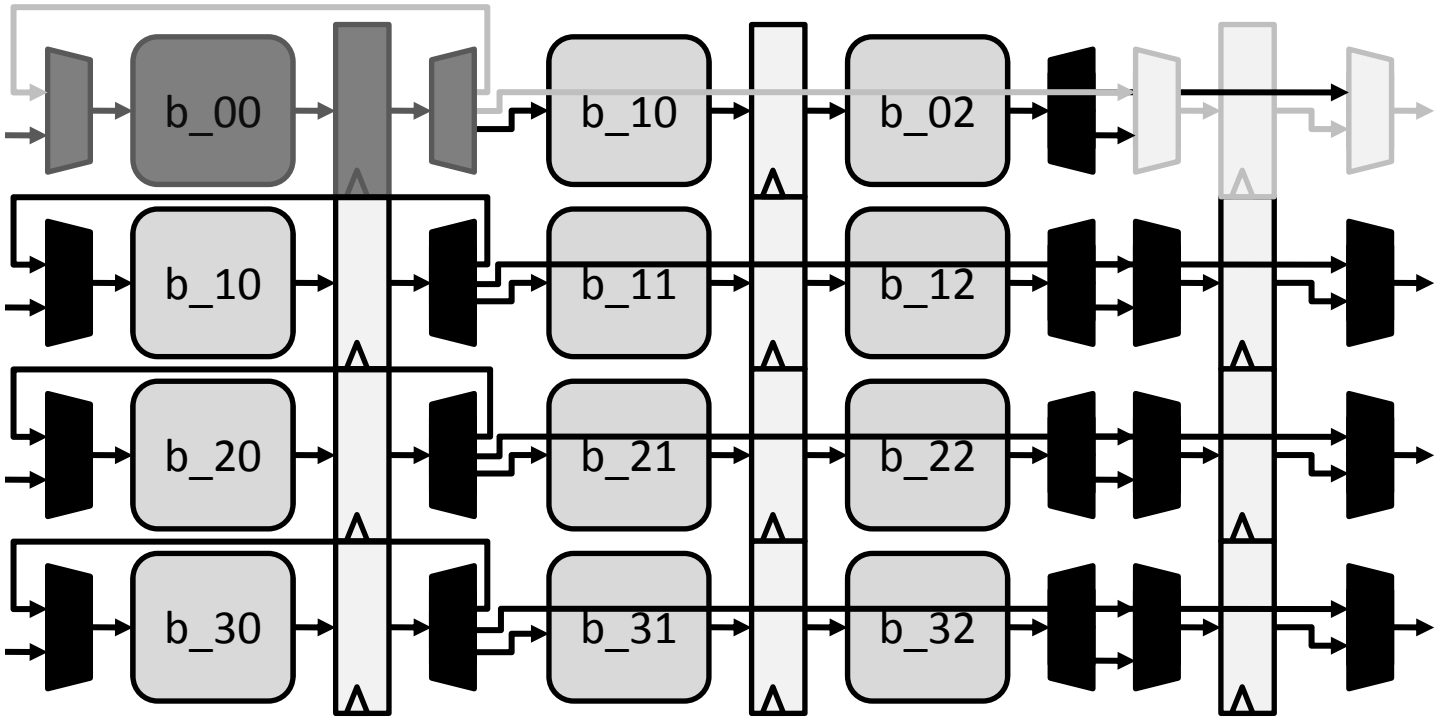


Dynamic Trade-off Management

Automatically Derived and Optimized FFT



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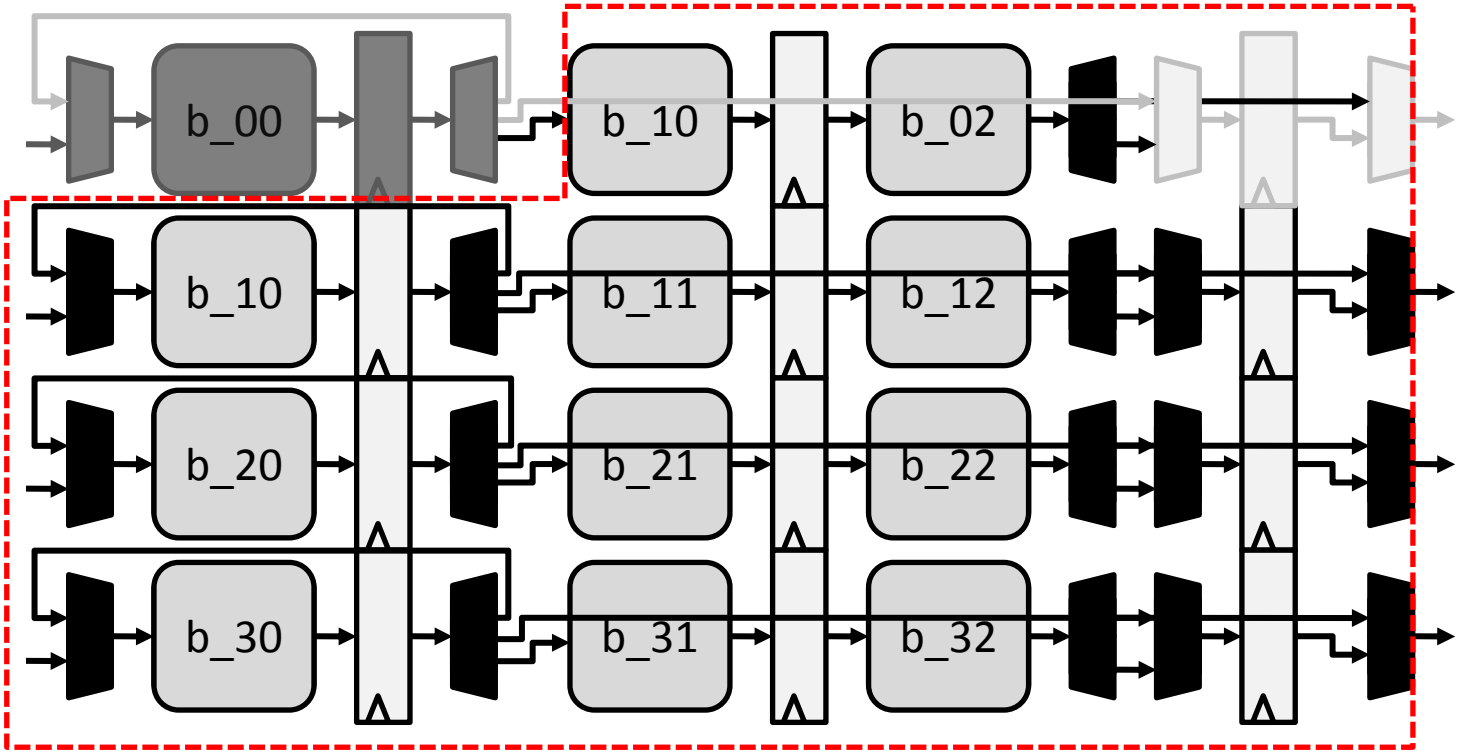

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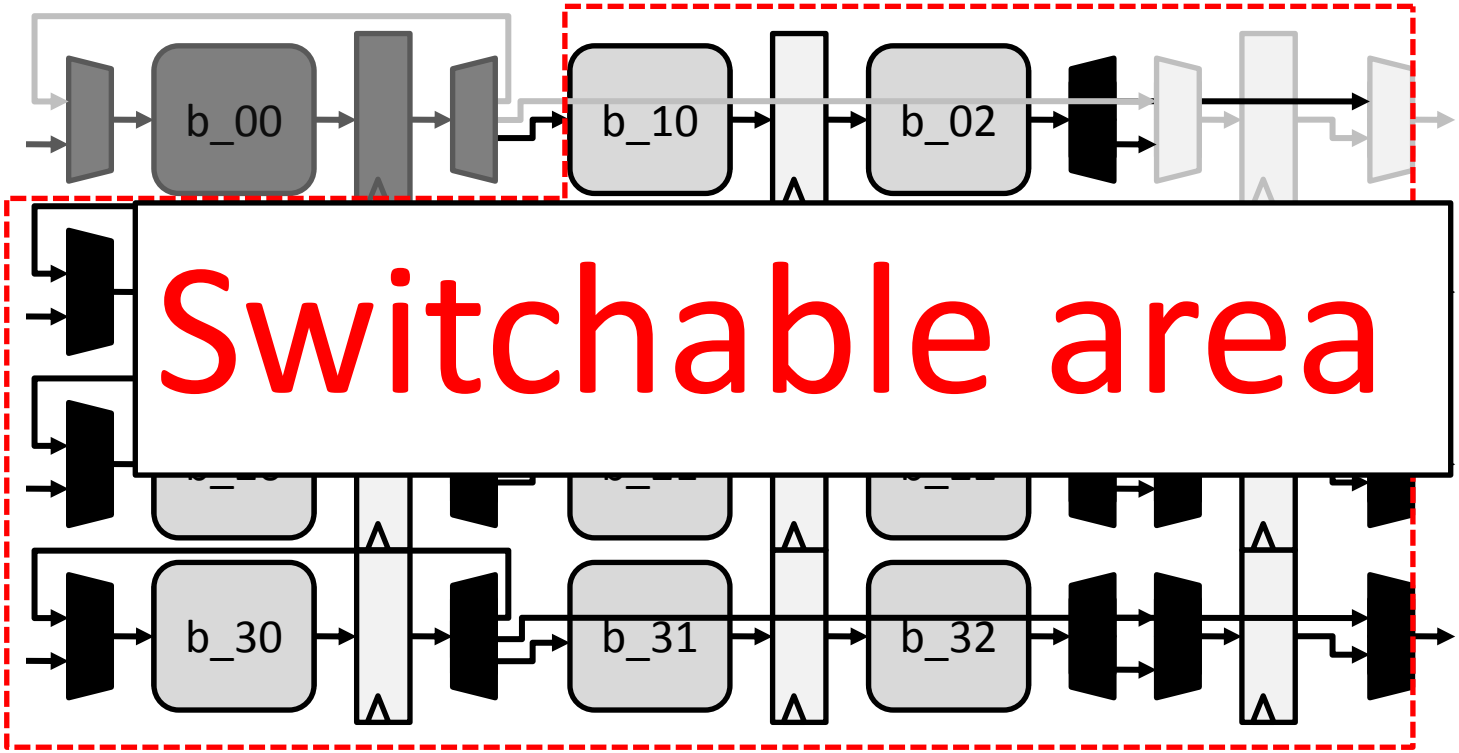

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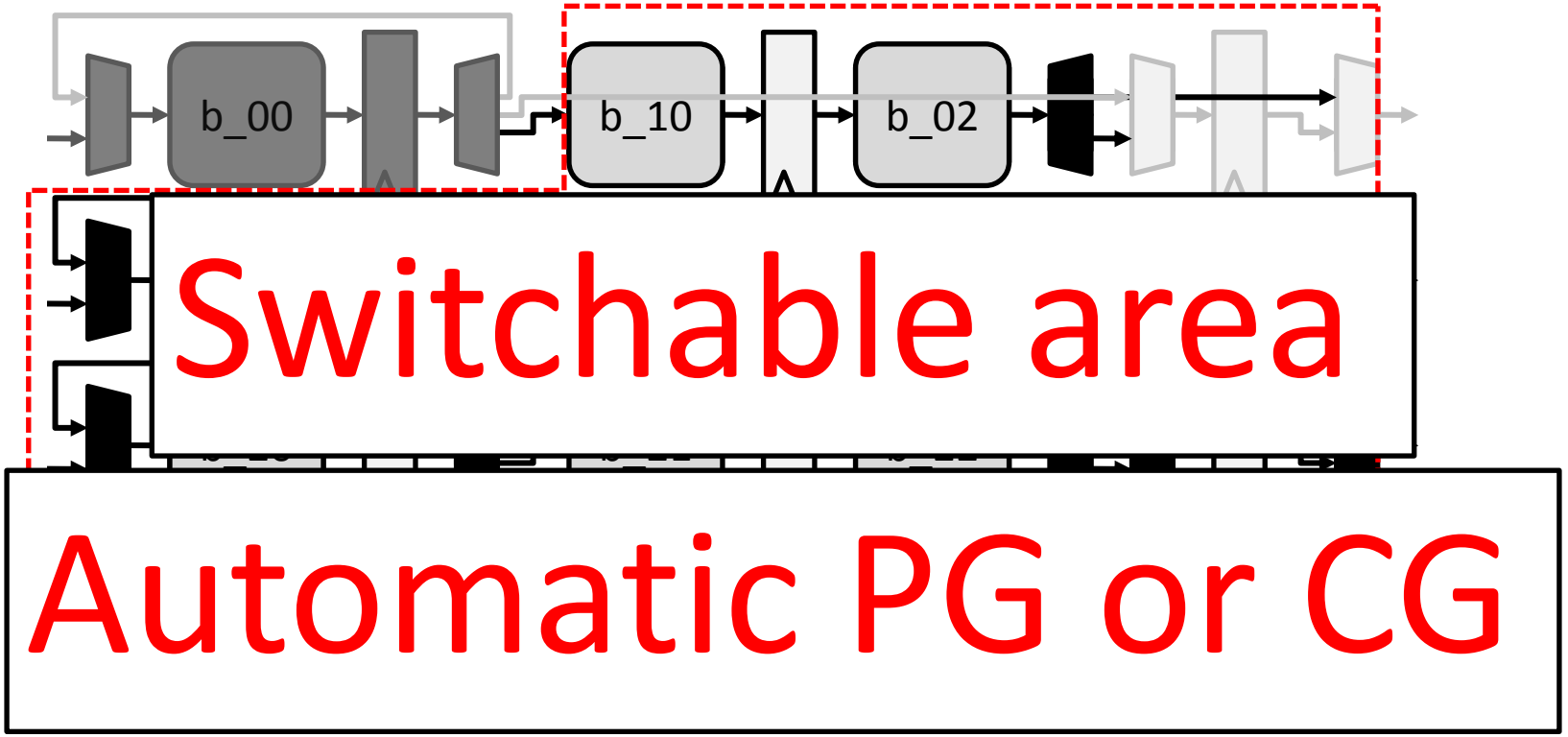

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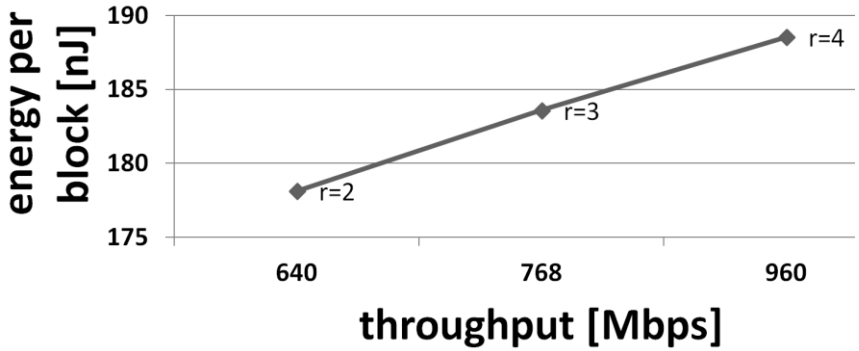
AES on Artix-7 FPGA



CGR AES-128: energy vs throughput

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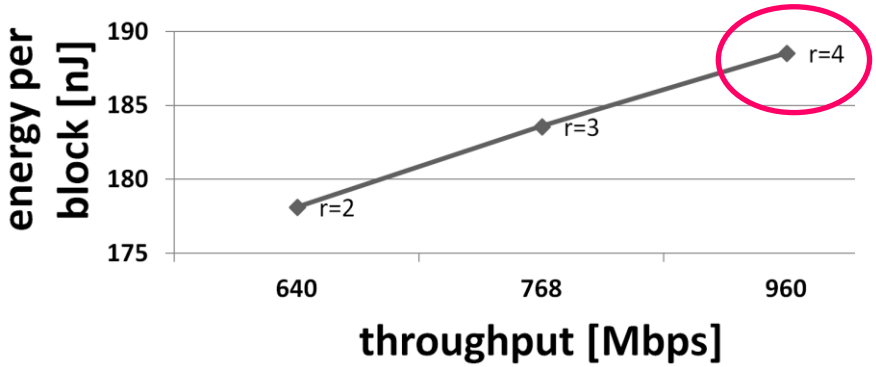

CGR AES-128: energy vs throughput

- r = 4
  - less energy efficient ciphers
  - maximum throughput → high performance applications (video stream encryption)

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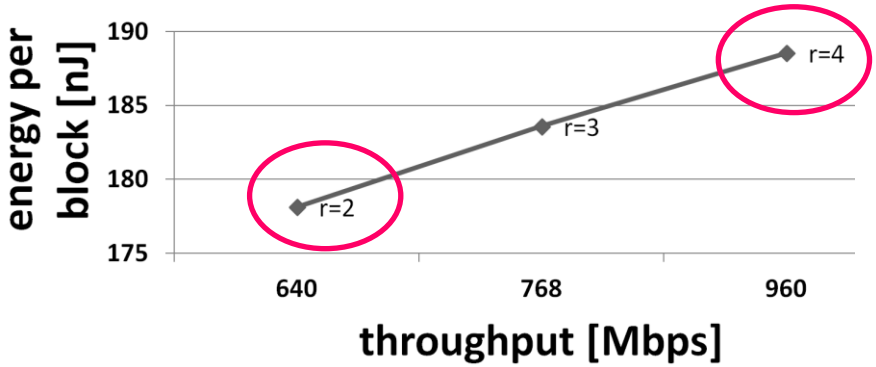
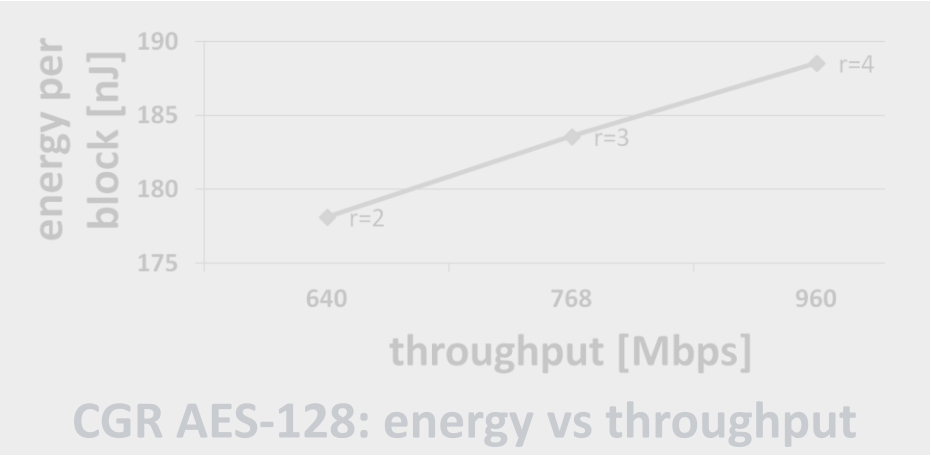


CGR AES-128: energy vs throughput

- r = 4
  - less energy efficient ciphers
  - maximum throughput → high performance applications (video stream encryption)
- r = 2
  - more energy efficient ciphers
  - slower execution → less computational demanding tasks (communicating with a RFID)

HEVC on Artix-7 FPGA



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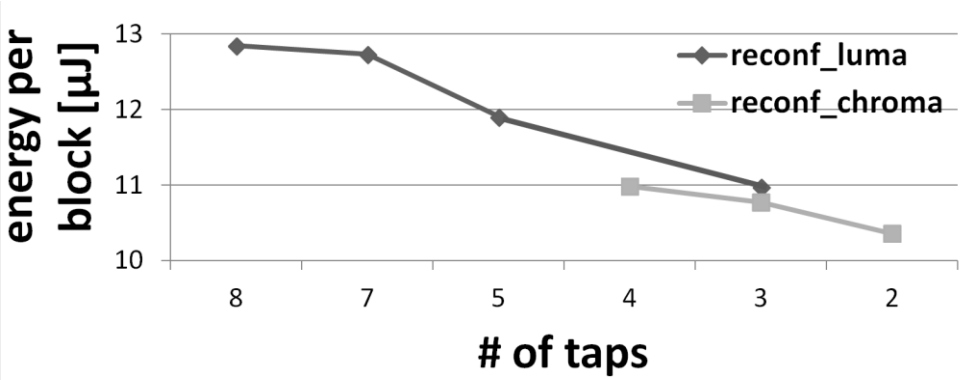
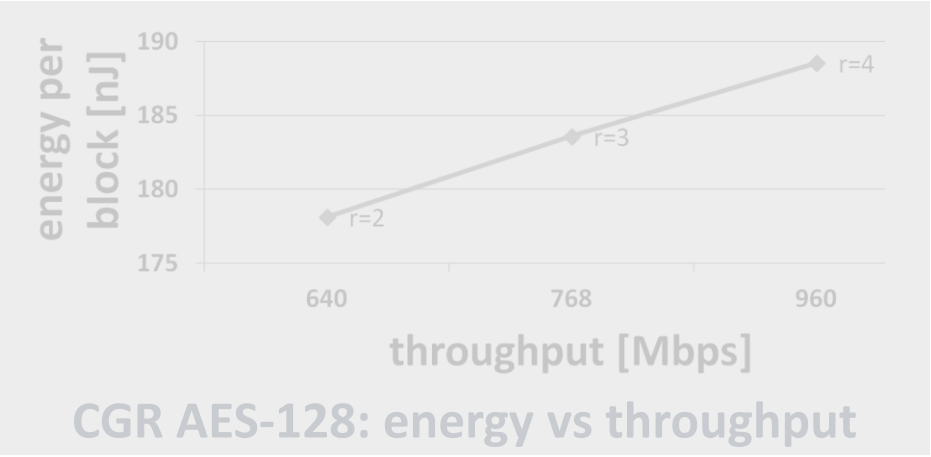
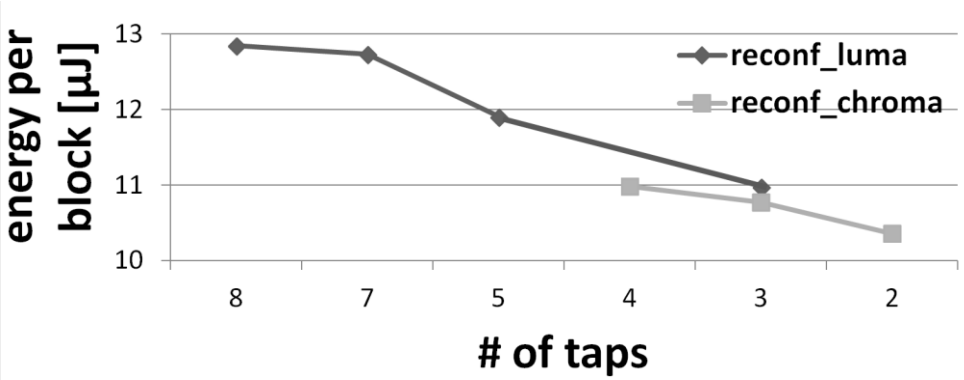


HEVC: energy vs quality

HEVC on Artix-7 FPGA



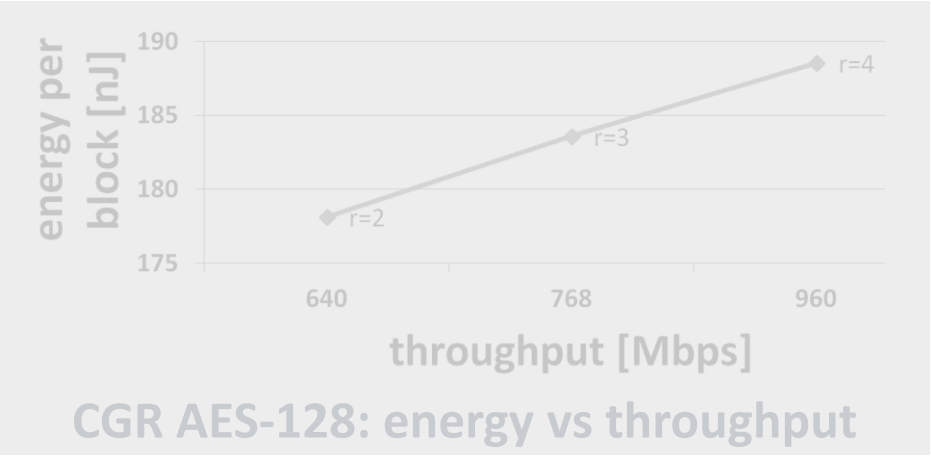
CGR AES-128: energy vs throughput



HEVC: energy vs quality

- High Profile – 8 taps luma and 4 taps chroma
  - High quality → higher energy

HEVC on Artix-7 FPGA



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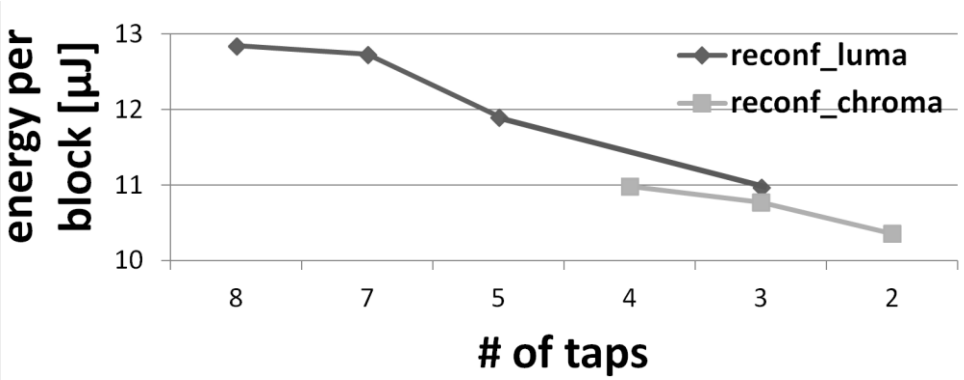
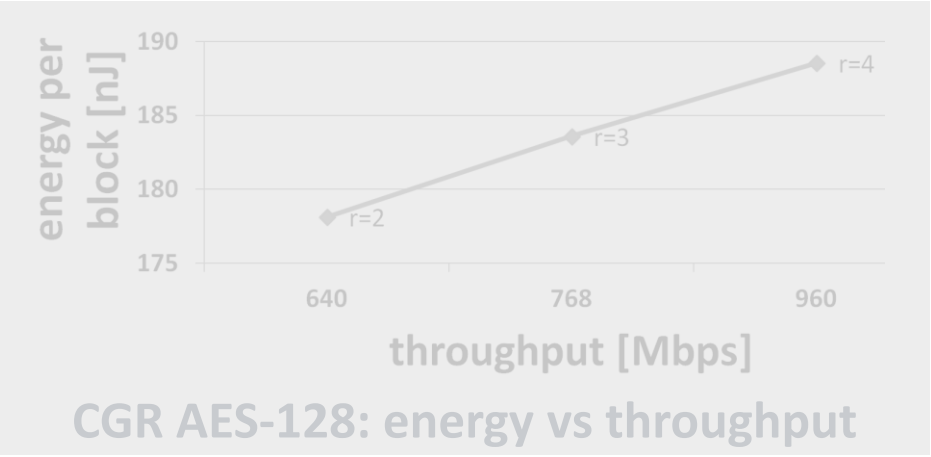


HEVC: energy vs quality

- High Profile – 8 taps luma and 4 taps chroma
  - High quality → higher energy
- Low Profile – 3 taps luma and 2 taps chroma
  - Lower quality → lower energy → **saves up to 15% luma and 5% chroma**

HEVC on Artix-7 FPGA



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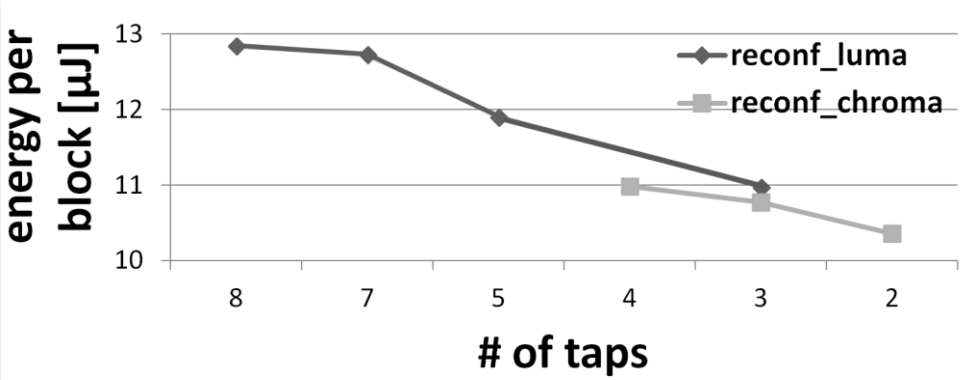

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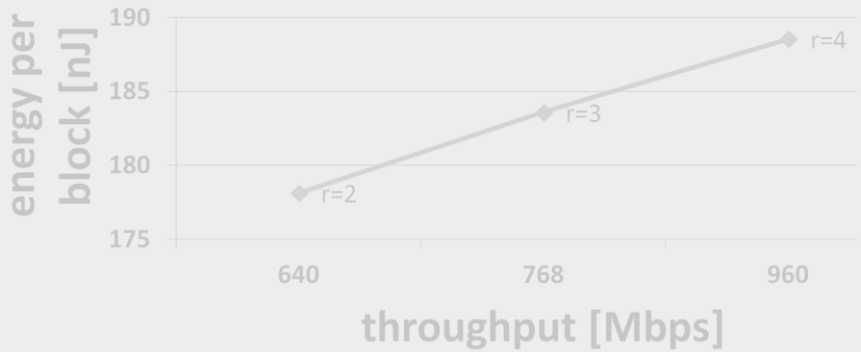
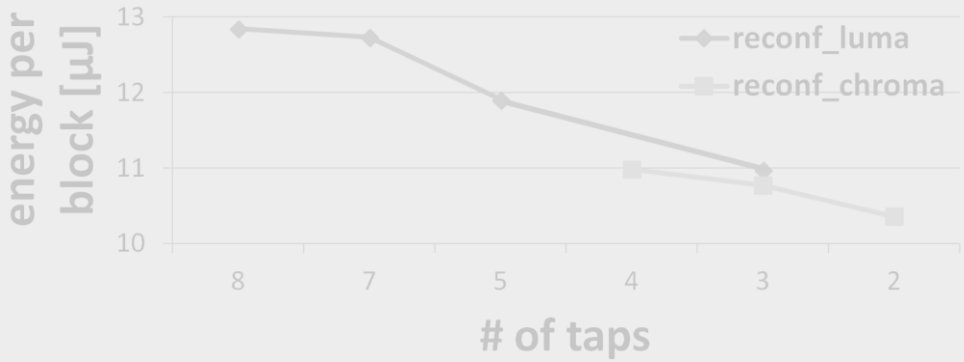
Even adopting a completely automated flow dynamic trade-off management can be still offered!

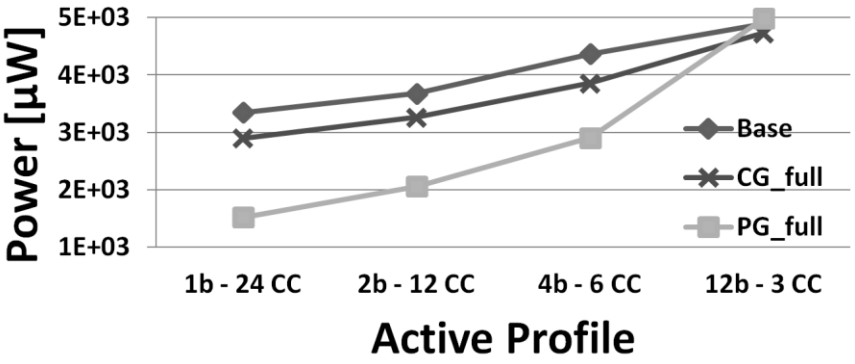
FFT on ASIC 90nm



CGR AES-128: energy vs throughput

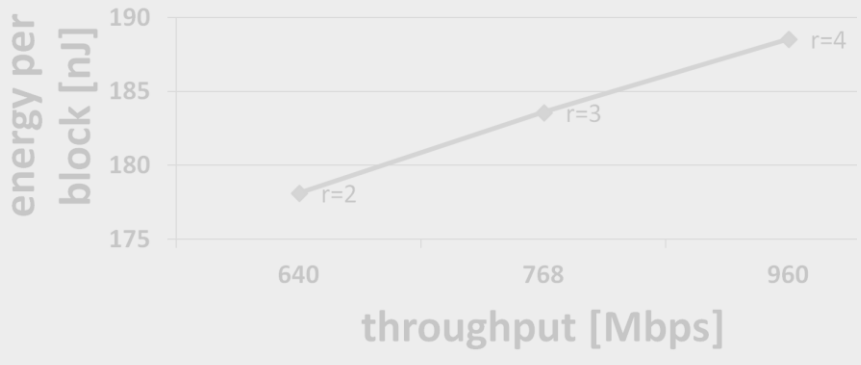


HEVC: energy vs quality

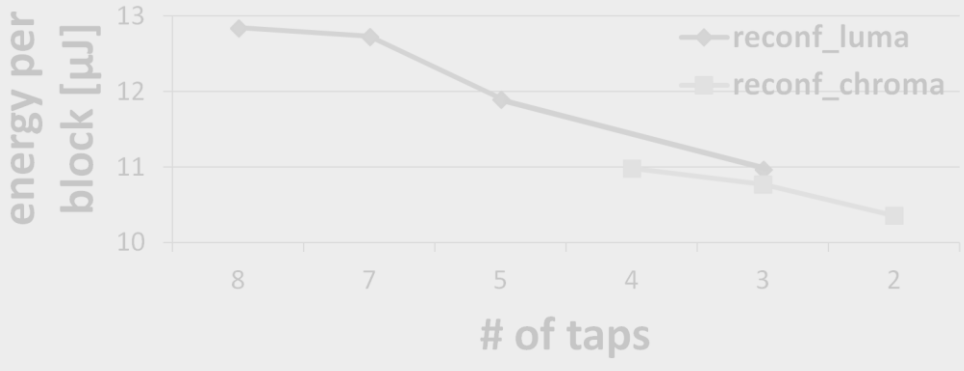


FFT: power vs throughput

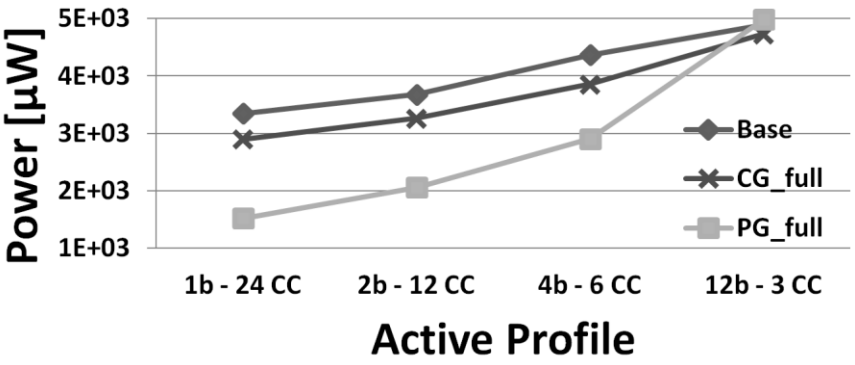
FFT on ASIC 90nm



CGR AES-128: energy vs throughput



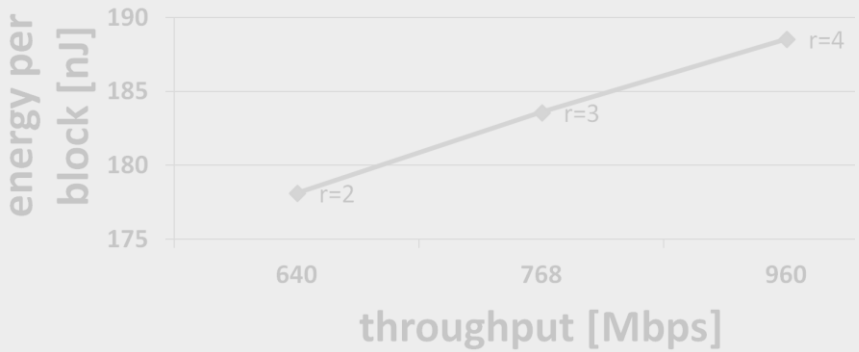
HEVC: energy vs quality



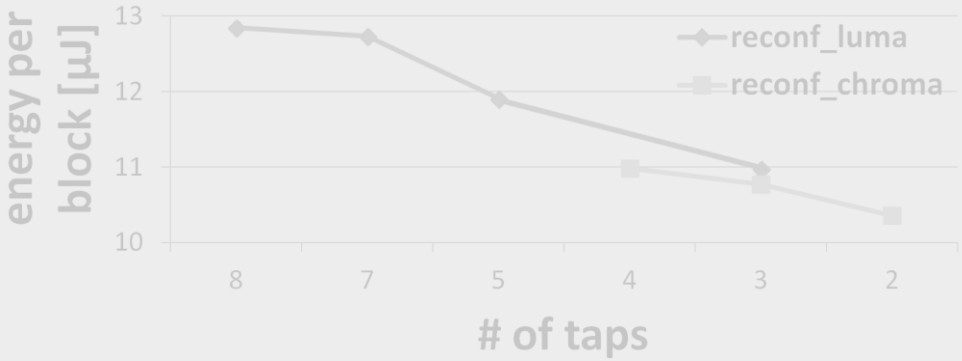
FFT: power vs throughput

Dynamic trade-off management is Confirmed on ASIC

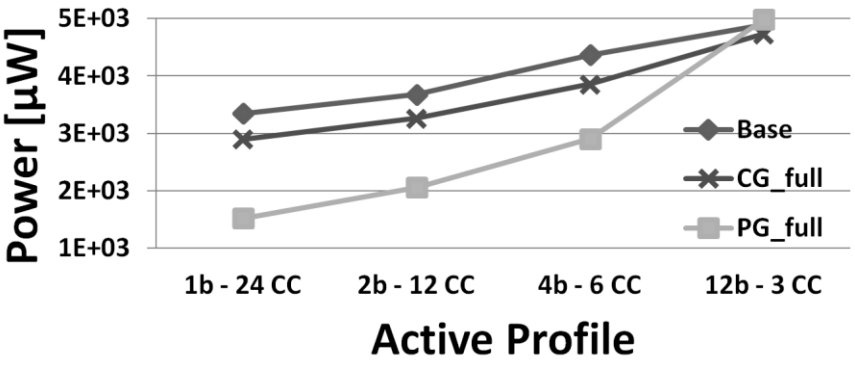
FFT on ASIC 90nm



CGR AES-128: energy vs throughput



HEVC: energy vs quality

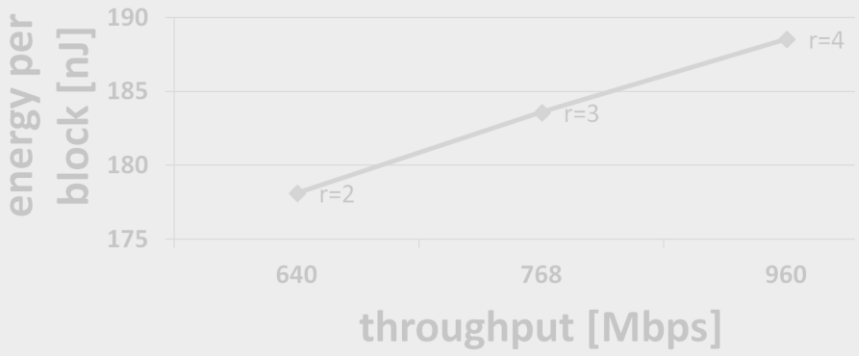


FFT: power vs throughput

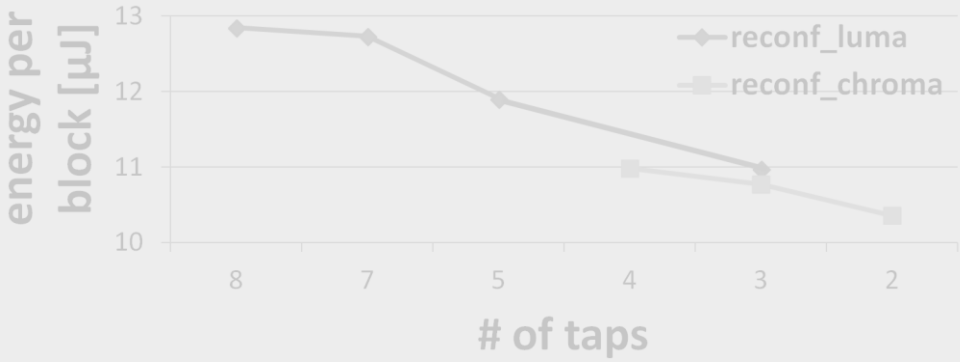
Dynamic trade-off management is Confirmed on ASIC

On ASIC MDC offers automatic implementation of power-gated and clock-gated designs

FFT on ASIC 90nm



CGR AES-128: energy vs throughput



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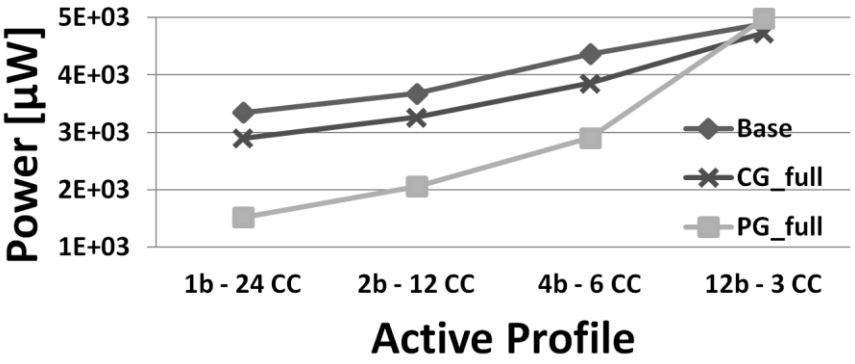


FFT: power vs throughput

	Area [GE]	vs Base%
Base	885575	---
CG_full	885871	0.03
PG_full	926835	4.66

FFT: Area

Outline

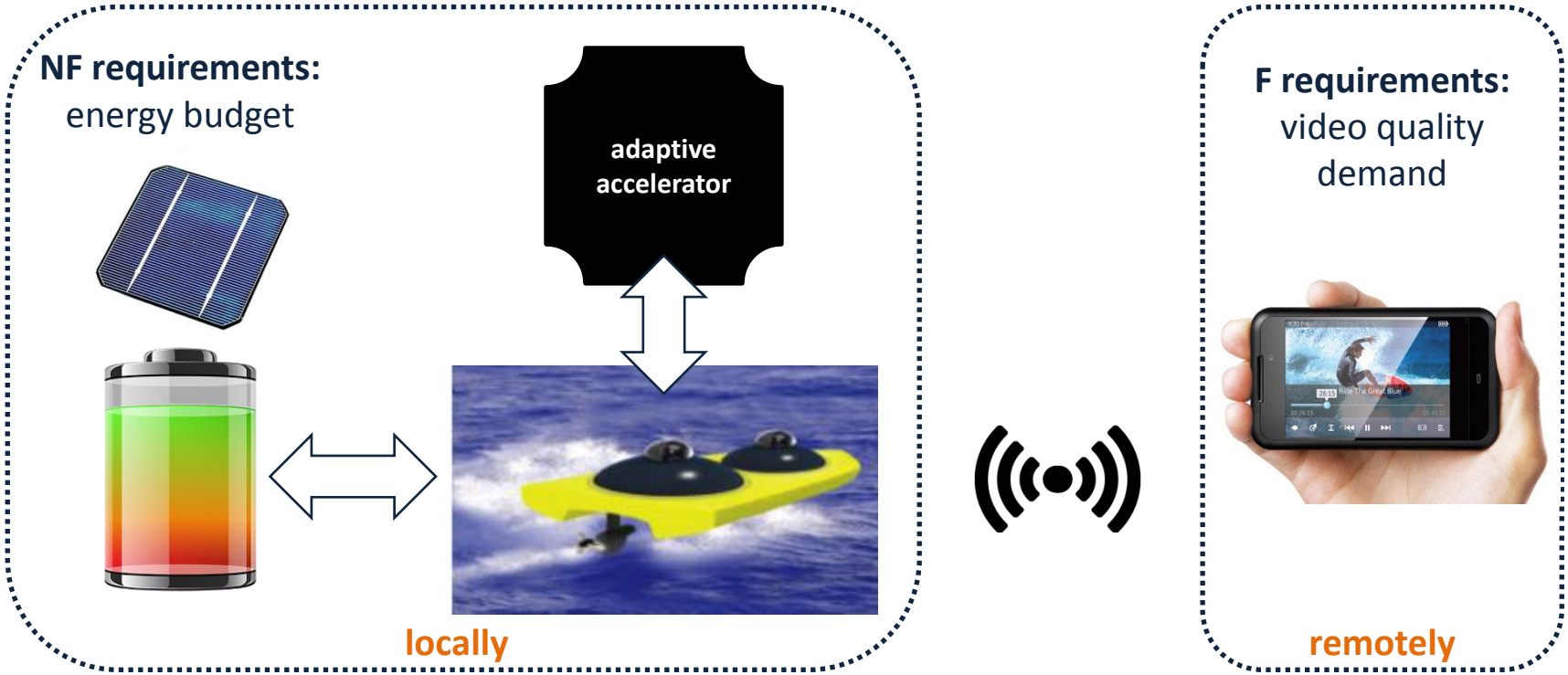
- Introduction
  - *Cyber Physical Systems*
  - *Coarse-Grained Reconfiguration*
  - *Multi-Dataflow Composer tool*
- Dynamic Trade-off Management
  - *Manually implemented CGR AES on FPGA*
  - *Automatically Derived HEVC interpolator on FPGA*
  - *Automatically Derived and Optimized FFT on ASIC*
- Experimental Results
- Conclusions

Conclusions

- **Cyber Physical Systems** require high performance and flexibility, with low energy consumption.
- **Coarse-Grained Reconfiguration** (CGR) allows high run-time adaptivity.
- **Dynamic trade-off management** has been achieved also with **automated design strategies** without any particular need of manual tuning.
- These results will be used as a starting point for the **EU Project CERBERO**

Future Directions

At the CPS physical level **application specific efficient accelerators** capable of providing **flexibility and dynamic adaptation to changeable F/NF requirements**.



Acknowledgements

The CERBERO project has received funding from the EU Commission's H2020 Programme under grant agreement No 732105.

Applications in Electronics Pervading Industry, Environment and Society

ApplePies2017

Challenging CPS Trade-Off Adaptivity with Coarse-Grained Reconfiguration

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21-22 September 2017 – Rome (IT)