49th Annual Meeting of the Associazione Società Italiana di Elettronica

SIE2017

Coarse-Grained Reconfiguration: Run-time Adaptivity in Cyber Physical Systems

Francesca Palumbo[1], **Carlo Sau[2]**, Paolo Meloni[2], Luigi Raffo[2]

[1]Università degli Studi di Sassari, PolComIng

[2]Università degli Studi di Cagliari, DIEE

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Outline

- Introduction
  - CERBERO and Cyber Physical Systems
  - HEVC Codec and Software Approximate Computing
- Approximate HEVC interpolators
  - Coarse-Grained Reconfiguration
  - From CG HEVC Interpolators to CGR HEVC Interpolators
- Results
  - Achieved Adaptivity
  - Comparison with the State of the Art
- Conclusions

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CERBERO project

Cross-layer mod**E**l-based framewo**R**k for multi-o**B**jective d**E**sign of **R**econfigurable systems in unce**R**tain hyb**R**id envir**O**nments

→ continuous design environment for **Cyber-Physical Systems (CPS)** including modelling, deployment and verification

http://www.cerbero-h2020.eu/

Self-healing system for planetary exploration

Smart Travelling for Electric Vehicle

Oceans Monitoring

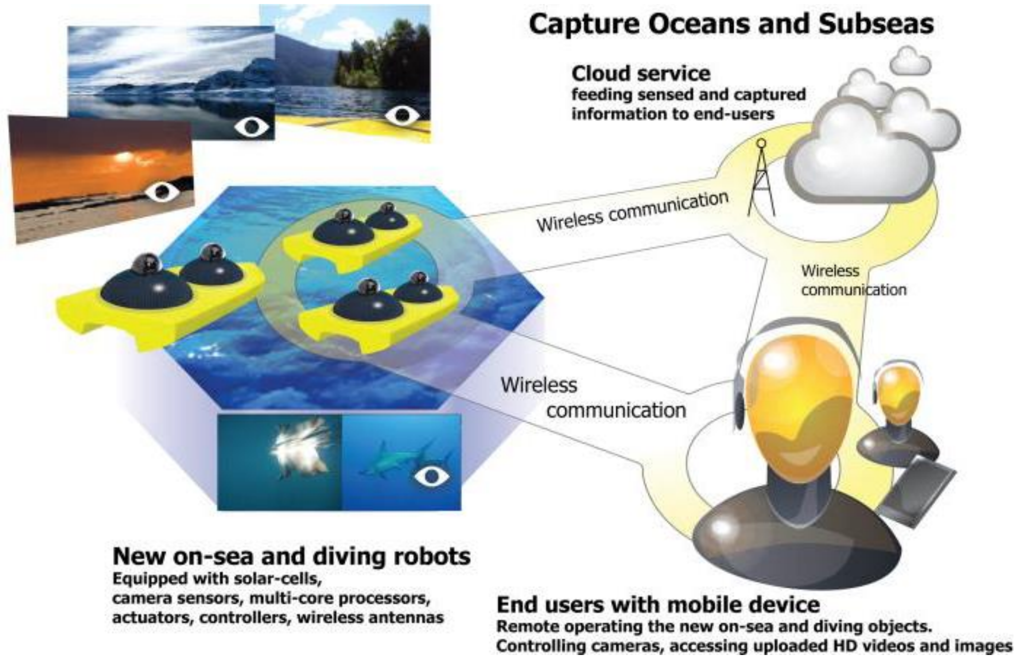
Cyber Physical Systems (CPS)

Complex systems with **different interacting and deeply intertwined components**, providing multiple and distinct **behavioral modalities** potentially **changing over time**, that contribute **concurrently** to determine the behavior of the system as a whole.

Layers (dominat aspects):

- functional
- physical
- communication

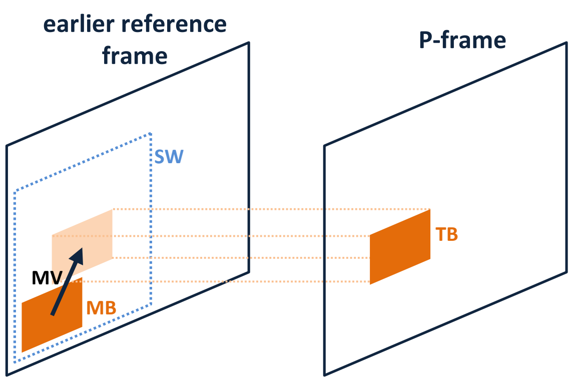
Subjected to **Functional** (F) and **Non-Functional** (NF) requirements variation in time.



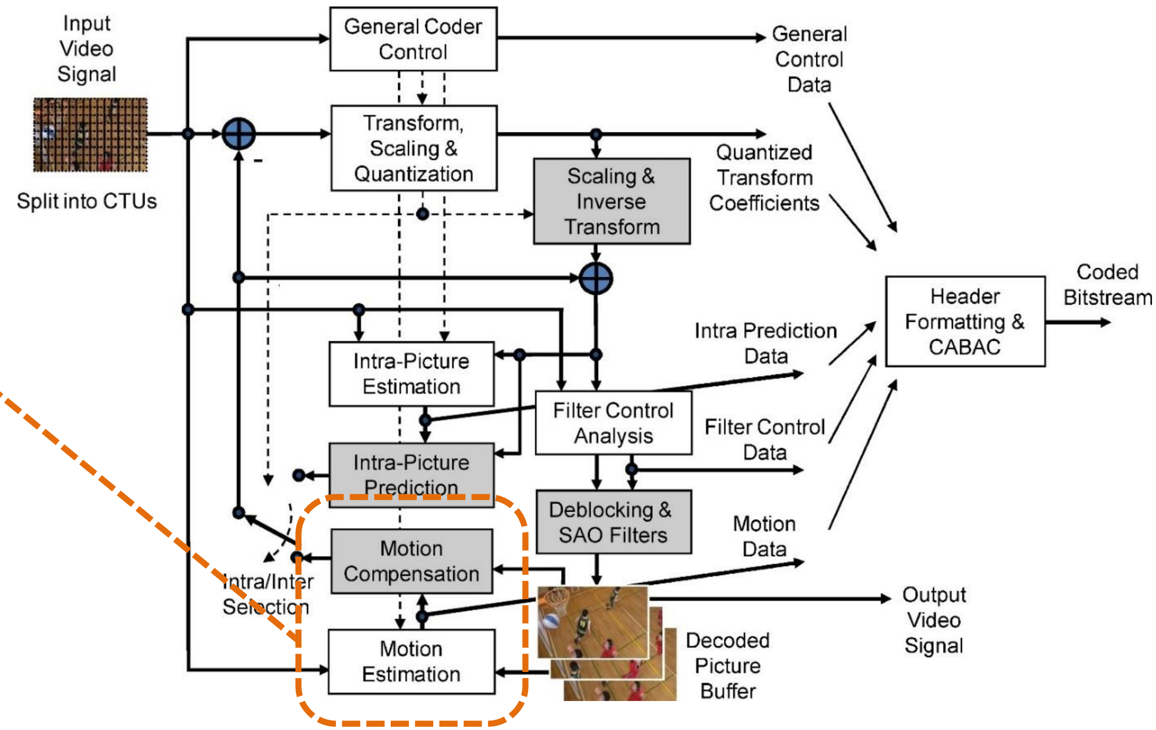
High Efficiency Video Coding (HEVC)

Recent video codec developed by the Joint Collaboration Team on Video Coding (VCEG and MPEG). It provides up to **50% bit rate reduction at the same subjective video quality** with respect to previous standards (H.264).

Computational Intensive and Power Hungry Step: Motion Estimation and Compensation

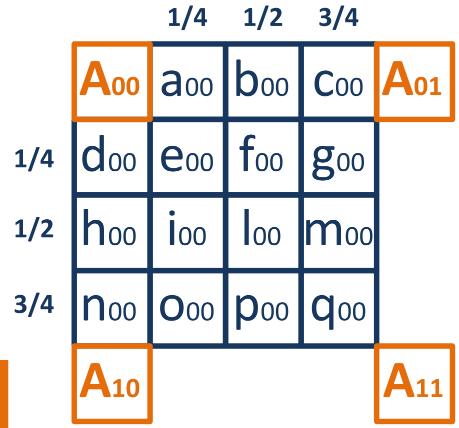


TB = target block
MB = matching block
SW = search window
MV = motion vector



Approximate HEVC Interpolation in Software

With high frame rates the **motion vector** could be composed of **fractional pixel** values. In these cases an **interpolation (FIR filtering)** of the matching block is necessary.



luma MV α	legacy	approximate [1]			
	8/7 tap	7 tap	5 tap	3 tap	1 tap
1/4, 3/4	-1, 4, -10, 58, 17, -5, 1	-1, 4, -10, 58, 17, -5, 1	1, -6, 20, 54, -5	-4, 20, 48	64
1/2	-1, 4, -11, 40, 40, -11, 4, -1	-1, 4, 11, 40, 40, -11, 3	2, -9, 40, 40, -9	-9, 41, 32	64

chroma MV α	legacy	approximate [1]		
	4 tap	3 tap	2 tap	1 tap
1/8, 7/8	-2, 58, 10, -2	-3, 62, 5	58, 7	64
1/4, 3/4	-4, 54, 16, -2	-5, 58, 11	50, 15	64
3/8, 5/8	-6, 46, 28, -4	-7, 51, 20	41, 23	64
1/2	-4, 36, 36, -4	-6, 42, 28	32, 32	64

→ up to **28% energy saving** with a **small degradation** of decoding quality on an ARM big.LITTLE SoC

[1] *E. Nogues et al., "Algorithmic-level approximate computing applied to energy efficient hevc decoding," IEEE Trans. On Emerging Topics in Computing, 2016.*

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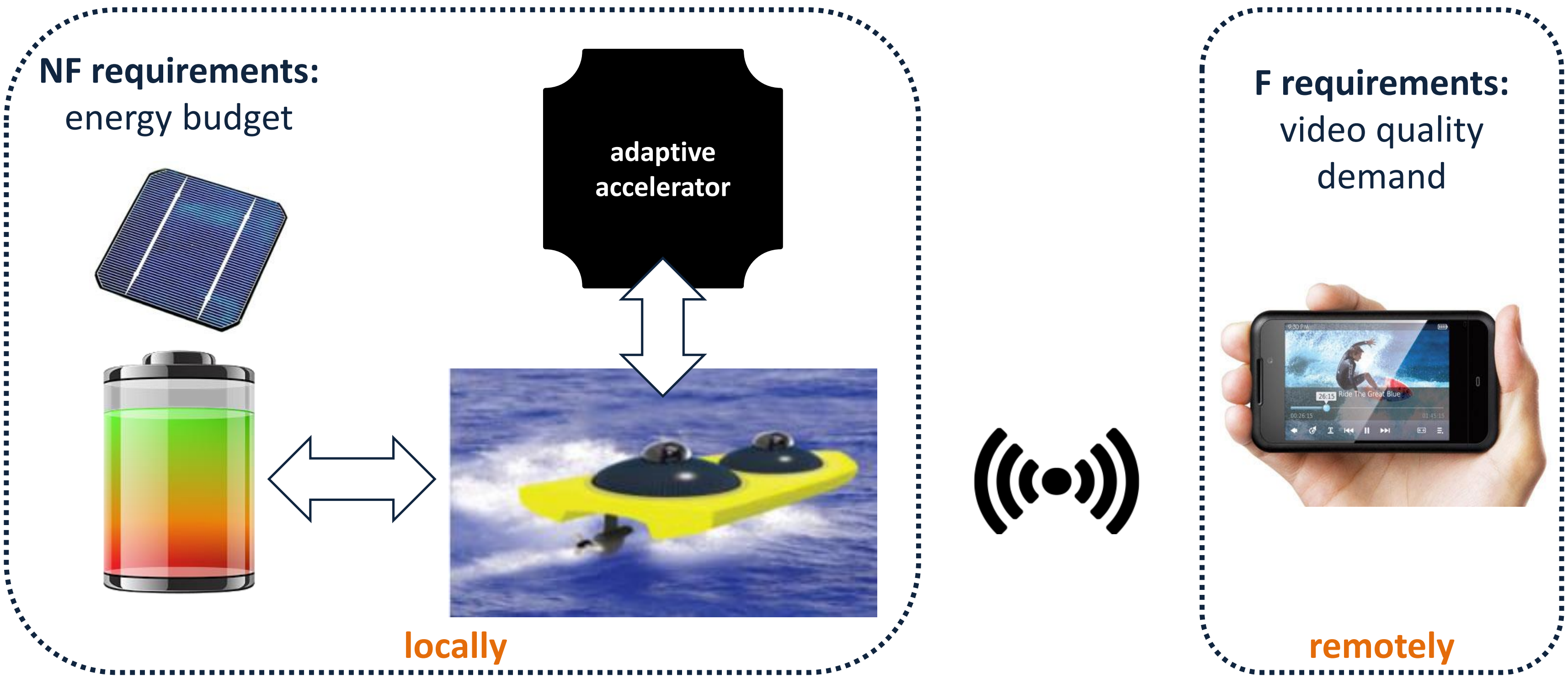
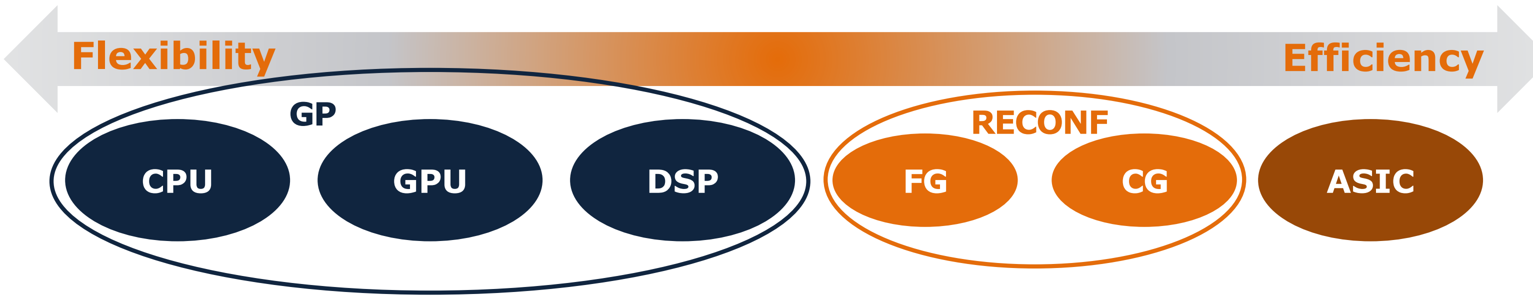
Run-time Adaptivity in CPS

At the CPS physical level **application specific efficient accelerators** capable of providing **flexibility and dynamic adaptation to changeable F/NF requirements**.



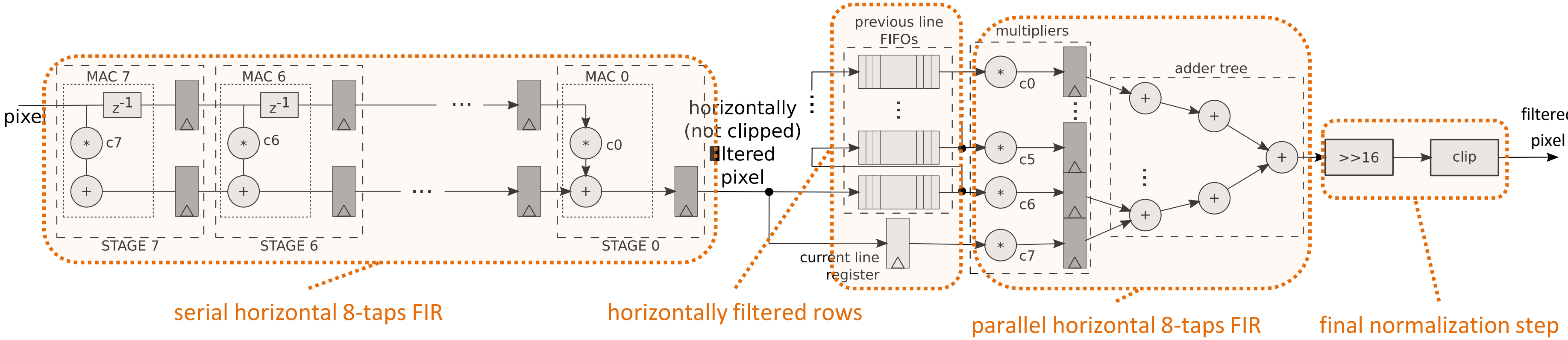
Coarse-Grained Reconfiguration (CGR)

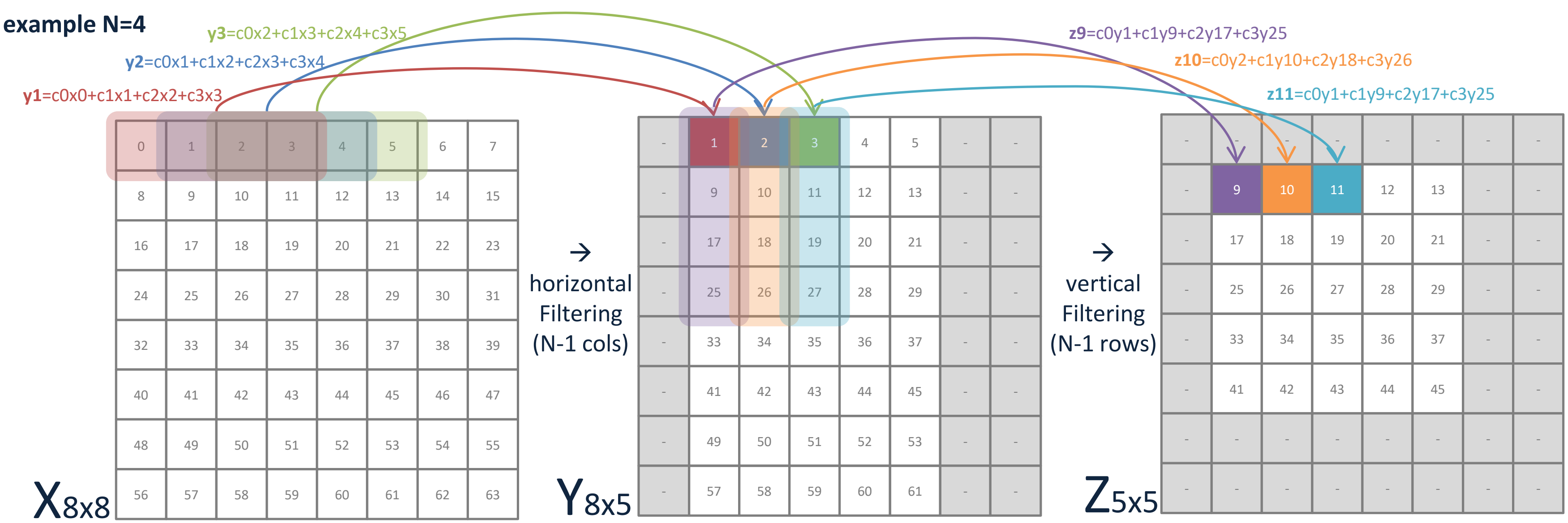


Reconfigurable computing provides a **trade-off between execution efficiency** typical of ASICs **and flexibility** mainly exhibited by GP devices.

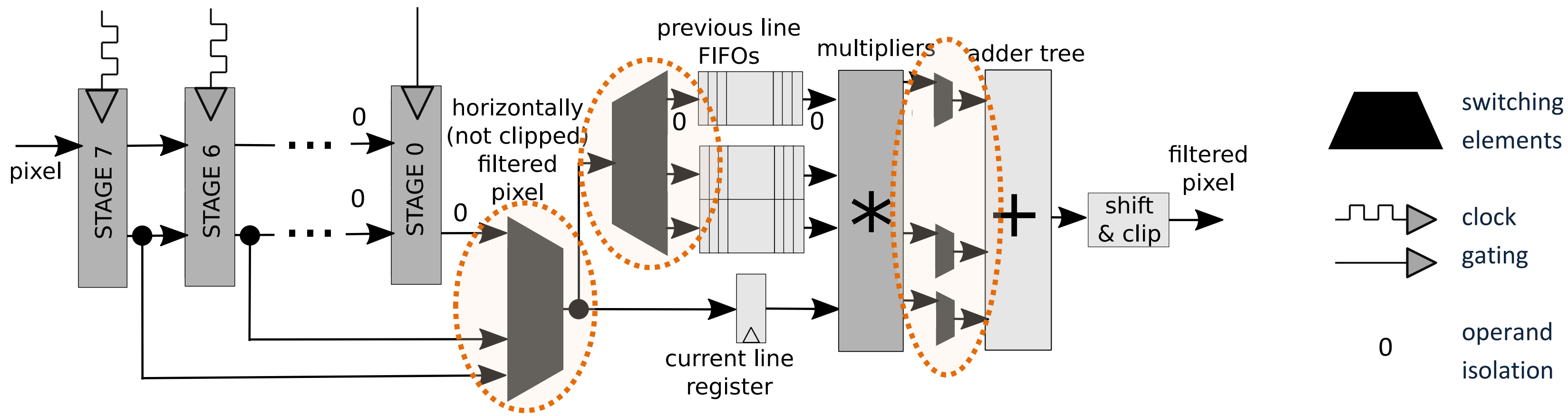
	Fine-Grained (FG) bit-level	Coarse-Grained (CG) word-level
flexibility	☺	😐
speed	😐	☺
memory	☹	😐

CG HEVC interpolators





CGR HEVC interpolators



profile	HIGH			MEDIUM			LOW		
	quality	# taps	energy	quality	# taps	energy	quality	# taps	energy
luma	☺	8/7	☹	😐	5	😐	☹	3	☺
chroma		4			3			2	

[2] *F. Palumbo et al., "Runtime energy versus quality tuning in motion compensation filters for HEVC," Proc. of the PDeS Conf., 2016.*

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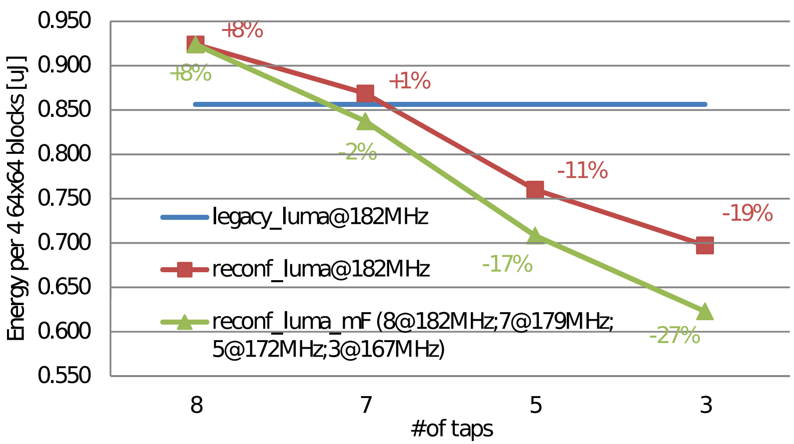
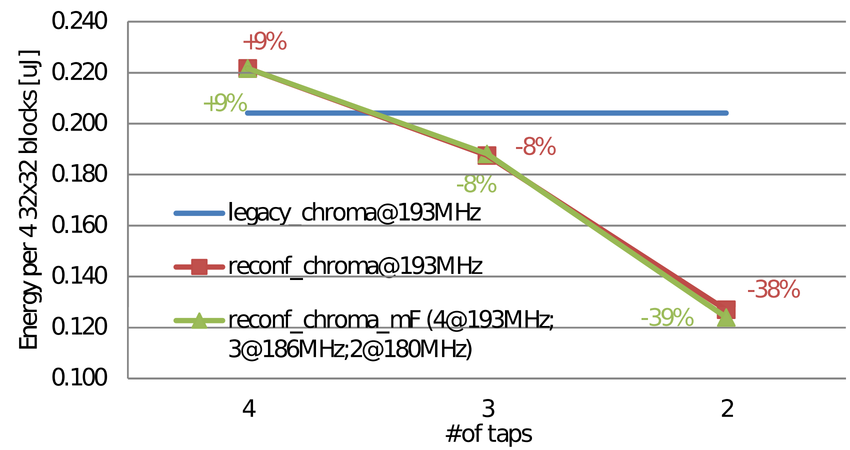
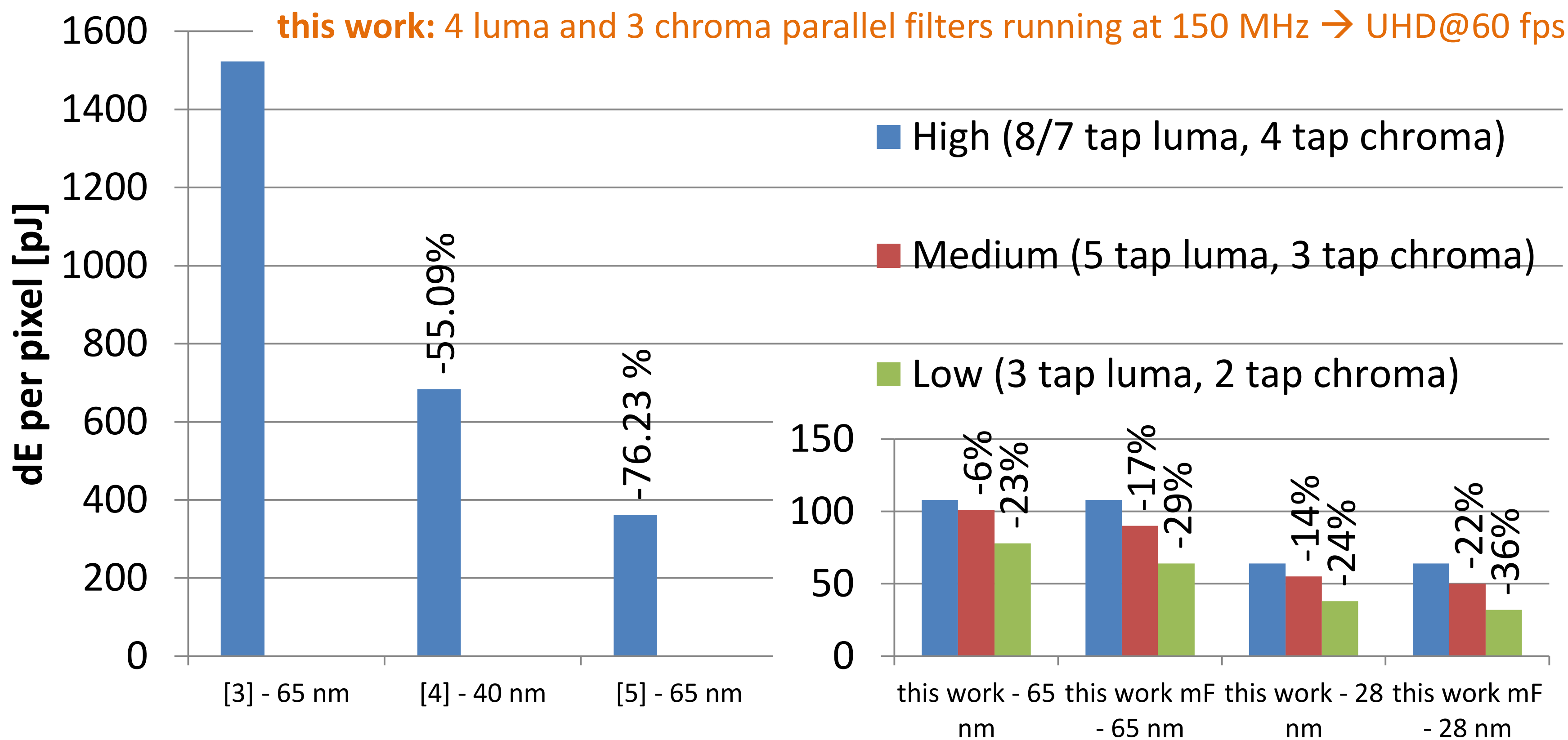
Achieved Adaptivity

design @200 MHz Xilinx XC7Z020	LUT	FF	BRAM	DSP	Fmax [MHz]	tap	dP (Vivado) [mW]	dE [µJ]	time per block [cycles]	# interpolated pixels in a fixed time
legacy_luma	212	37	4	16	213	8	11	0.248	460	57957
reconf_luma (vs legacy %)	582 **(+175%)**	85 (+130%)	4 (+0%)	16 (+0%)	200 **(-6%)**	8	12 (+9%)	0.270 (+9%)	460 (+0%)	57957 (+0%)
						7	11 (+0%)	0.245 (-1%)	395 (-14%)	59033 (+2%)
						5	10 (-9%)	0.217 (-12%)	265 (-42%)	61191 (+6%)
						3	10 **(-9%)**	0.211 **(-15%)**	135 **(-71%)**	63357 **(+9%)**
legacy_chroma	163	33	2	8	217	4	9	0.053	107	14753
reconf_chroma (vs legacy %)	383 **(+135%)**	65 (+97%)	2 (+0%)	8 (+0%)	200 **(-12%)**	4	9 (+0%)	0.053 (+0%)	107 (+0%)	14753 (+0%)
						3	8 (-11%)	0.045 (-13%)	73 (-32%)	15293 (+4%)
						2	6 **(-33%)**	0.033 **(-37%)**	39 **(-64%)**	15835 **(+7%)**





Comparison with the State of the Art



[3] V. Afonso et al., "Low cost and high throughput FME interpolation for the HEVC emerging video coding standard," Proc. of the IEEE LASCAS Conf., 2013.

[4] E. Kalali et al., "A reconfigurable HEVC sub pixel interpolation hardware," Proc. of the IEEE ICCE Conf., 2013.

[5] C. M. Diniz et al., "A reconfigurable hardware architecture for fractional pixel interpolation in high efficiency video coding," IEEE Comput.-Aided Des. Integr. Circuits Syst., vol. 34, no. 2, pp. 238–251, 2015.

Outline

Conclusions

- **CERBERO**: continuous design environment for **Cyber-Physical Systems** (CPS)
  - run-time F/NF requirements driven adaptivity
- **HEVC** power/energy hungry, latest video coding standard
  - **Approximate computing** on HEVC interpolators demonstrated to provide energy versus quality trade-off
- **Coarse-Grained Reconfiguration** (CGR) allows approximation of HEVC interpolators in hardware
  - our solution challenges outperforms state of the art solutions

- Future directions on:
  - adopt a **multiplier-less** solution to further reduce consumption
  - embedding the **whole HEVC codec on FPGA** (software/hardware)

CPS Summer School 2017

Porto Conte Ricerche, Alghero (Italy) – September 25-30, 2017

Designing Cyber-Physical Systems – From concepts to implementation

Multi-objective Methodologies and Tools for Self-healing and Adaptive Systems

Distinguished lecturers: Alberto Sangiovanni-Vincentelli, Hironori Kasahara, Muhammad Shafique

Application deadline: **July 7th, 2017**

http://www.cpsschool.eu/

Acknowledgements

The CERBERO project has received funding from the EU Commission's H2020 Programme under grant agreement No 732105.

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Carlo Sau

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carlo.sau@diee.unica.it

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