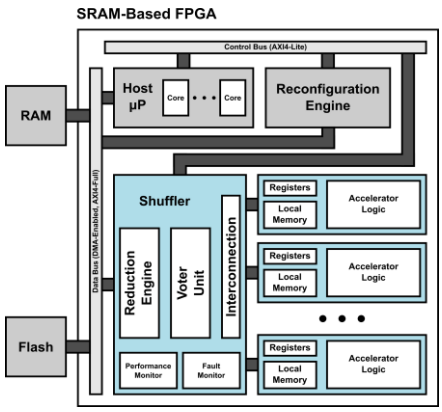
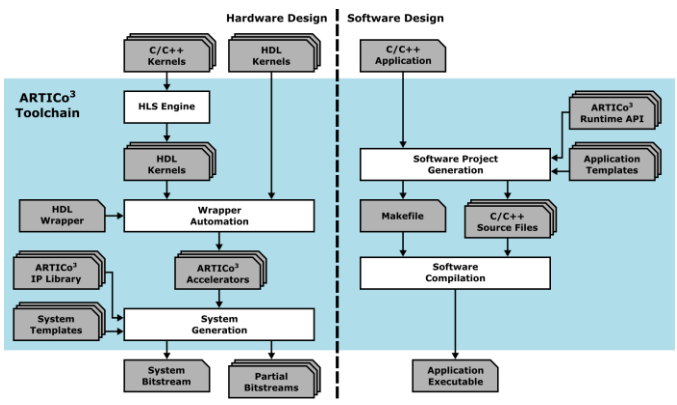
Users	• Embedded system designers with no prior knowledge/expertise in hardware development or partial reconfiguration techniques • Embedded system designers targeting applications with dynamically (i.e., at runtime) changing requirements of computing performance, energy consumption and fault tolerance • Embedded system designers targeting applications with stringent availability requirements
Key Features	• Run-time adaptive, DPR-enabled hardware processing architecture with flexible datapath to support different accelerator configurations • Integrated development flow, ranging from application specification (design time) to application execution (run time) • Automated toolchain to hide low-level DPR details (floorplanning, design partitioning) in Xilinx FPGAs **DPR – Dynamic and Partial Reconfiguration*
Benefits for the User	• Transparent management of Dynamically and Partially Reconfigurable systems at both design- and run-time for end users • Transparent offloading of data-parallel applications onto a configurable number of energy-efficient, fault-tolerant hardware accelerators
Inputs	• Host Application Code: C/C++ code describing the SW application that runs in a host processor. Requires specific API function calls (included in the framework) to use the HW-based coprocessor infrastructure. • Kernel Code: C/C++ code when using High Level Synthesis (HLS), HDL code otherwise, that describes the computing-intensive, data-parallel functionality to be accelerated using dedicated reconfigurable HW resources.
Outputs	• FPGA Configuration Files: binary files containing the information required to program the implemented digital circuits in the target device. The tool chain generates configuration files for both static region (i.e. does not change during circuit operation) and reconfigurable partitions (i.e. each slot, which can be modified at runtime). • Application Executable: binary file that runs in the host processor, offloading the computing-intensive and data-parallel operations to the hardware accelerators available in the FPGA.
Block Design	*ARTICo³ architecture*  *ARTICo³ toolchain* 
Role in the Toolchain	Hardware adaptation with DPR-enabled scalable/fault-tolerant/energy-efficient acceleration